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Single-Phase Nonlinear Power Electronic Loads: Modeling and Impact on Power System Transient Response and Stability

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Single-Phase Nonlinear Power Electronic Loads: Modeling and Impact on Power System Transient Response and Stability

by

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Dedication

I would like to thank my family and friends for their love and support as I completed my Ph.D. I appreciate my parents support and encouragement throughout my academic pursuit. I am especially grateful for the love and support from Lori Murphy. She has been by my side the whole way through. I would also like to thank my supervisor W. Mack Grady and Ari Arapostathis for the interesting topic and guidance they have given me over the past four years. They have made my graduate research an educational and enjoyable experience. Finally, I would like to thank my dog Maxwell. For the past two years, whenever I needed a distraction, he was always there.

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This dissertation examines single-phase nonlinear power electronic loads. The transient response of power electronic loads is unlike traditional linear loads. Therefore, a composite power electronic transient load model is developed. The load model dynamics are validated with actual utility voltage sag response data, laboratory controlled load response testing, and power electronic load dynamic simulations. The power electronic load model is applied in the University of Texas at Austin power system. The system transient response is unique and considerably different from what it would be with traditional linear loads. The power electronic load can be friendly or unfriendly to the system depending on the fault and system configuration.

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Chapter 1 – Introduction

Power system stability studies are only as accurate as the models used to represent the system. In today's society, these models continue to change as new equipment and loads are brought into the network. Typically, detailed models of source-side components have been constructed, but less has been done to improve the system composite load models.

Variables such as location, weather, season, and time of day have a significant impact on the system load composition and thus influence the composite load models. One method to determine the load composition and characteristics is the measurement-based procedure. This procedure requires actual power flow data for voltage and frequency variations which are typically measured from monitoring stations on low-side distribution transformers using power quality monitors or substation relays. The data are then fit to the appropriate load models to determine their characteristics.

The traditional and well accepted load model used in most transient stability programs depicts the load as if it is static. The static model well represents the majority of linear loads; however, the model is not well suited for single-phase nonlinear power electronic loads which usually make up at least 5% and often 10-15% of the present day residential MW demand.

Power electronic loads, such as televisions and computers, use a DC capacitor-filtered diode-bridge to rectify AC voltage. The DC capacitor causes the nonlinear load to momentarily disconnect from the system twice every power frequency cycle and longer during voltage sags. At voltage sag recovery, the power electronic load demands additional power compared to the previous steady state to recharge the DC capacitor. These dynamics are not represented by the traditional static load model and have led to the development of a new transient load model for power electronics. The power electronic load can have either a friendly or unfriendly affect on the transient response and stability of the power system.

DISSERTATION OVERVIEW

In Chapter 2, the dissertation gives a brief history of the power system and traditional load models. Several types of static and dynamic load models are discussed, however, the exponential load model is chosen as the most relevant for traditional linear loads.

Chapter 3 discusses a method for decomposing utility load using power flow data during and prior to naturally-occurring voltage sags which are particularly frequent during thunderstorms. The load is decomposed into linear and nonlinear power electronic components and then further examined to determine the linear active and reactive powers. The variation of the linear load due to the voltage sag is observed, and the best composite linear load models are determined. The procedure is supported with load response data from a hardware based Voltage Sag-Test Station [1] and with actual utility data from distribution feeders in Austin, TX. Results match well with commonly cited references and simulations.

In Chapter 4, I observe the harmonic properties of power electronic loads. Power electronic loads are rich in harmonic current distortion (THDi). THDi, however, is nonlinearly dependent with the load voltage harmonic distortion (THDv). I study the effects of THDv on THDi with a specially-developed Harmonics Testing Station. THDi is found to vary considerably with voltage harmonic magnitude and phase angle. Therefore, unlike previously thought, harmonic Norton equivalent models are not accurate for even mildly nonlinear loads.

Chapter 5 discusses the design of a transient power electronic load model for use in transient stability studies. The transient response of power electronic loads is dramatically different than that of linear loads. Power electronic loads trip offline during a fault when the system voltage drops suddenly, whereas linear loads remain online changing power demand by their governing characteristics and system voltage. Power electronic loads, however, do have the ability to come back online during the fault as their DC capacitors discharge. After the fault is cleared, the loads then demand additional power to recharge their load capacitors.

The transient model is developed using the analytical dynamics of individual power electronic loads and then adjusting for composite loads. The composite model describes the distributed transient response of the individual loads.

In Chapter 6, the power electronic dynamic equations are used to solve for the transient load model characteristics for 3125 simulated events. From the events, I determine trends and the most probable transient load model characteristics.

The Voltage Sag-Test Station is reused in Chapter 7, with minor improvements, to observe the actual transient response of power electronic loads. Using the actual load model parameters, the transient response characteristics are determined. The response of the composite power electronic load model is verified with the actual composite load response.

In Chapter 8, I determine the utility power electronic load model parameters and transient response characteristics using actual distribution feeder voltage sag data. The characteristics are used to implement the model in power system stability software.

The utility power electronic load is applied in the University of Texas at Austin power system stability model in Chapter 9. Large amounts of power electronic loads will cause the mechanical/electrical power imbalance to increase at the onset of a fault which accelerates the generators faster than the traditional load. If the power electronic load comes back online during the fault near the accelerating machines, the generators decelerate and the energy displaced by the DC capacitors is limited. The net effect is beneficial to power system stability. However, if the load does not come back online during the fault, the post-fault inrush is more significant and the net effect is adverse to system stability. The response of the power electronic load can lead to stability issues imperative to the power system. These effects can be friendly or unfriendly and depend on the fault and system configuration.

Chapter 10 concludes the research. The achievements of this dissertation are:

- A transient model for single-phase power electronic loads that is suitable for incorporation into transient stability studies of electric power grids.
- Transient load model validated with actual utility load, laboratory controlled load, and simulated load.
- Evaluation of the impact of power electronic loads on power system transient response and stability.
- Measurement-based procedure to
    - Decompose composite load into linear and power electronic components.
    - Determine traditional linear load characteristics.
- Relationship between voltage and current distortion of power electronic loads.
- Identification of the errors associated with the use of Norton equivalent models for power electronic loads.
- Development of:
    - System impedance monitoring station.
    - Harmonics testing station.
    - Voltage sag-test station.

Chapter 2 – Background on Power Systems and Traditional Load Models

The first complete American power system was built by Thomas Edison in 1882. This was a DC system comprised of a generator, cable, fuses, and an incandescent lamp load. There were, however, many disadvantages of the DC network including high line losses and considerable voltage drops. These disadvantages, which limited transmission length, led to the development of the AC system.

The AC system began in North America in 1886 after George Westinghouse secured the rights to the French scientists', L. Gaulard and J.D. Gibbs, work on the transformer and AC transmission system. In 1893, with the improvements to the AC system by Nikola Tesla, the advantages of the AC network ended the controversy between the AC and DC system standard. The AC system was at this point considered America's primary electrical network [2].

The first stability problems began to be recognized by the early 1920's [3]. At the time, the models and methods of analysis were limited by the theory of dynamic systems and computational tools such as slide rules and mechanical calculators. The first, simplistic, system model consisted of an ideal voltage source serving only constant impedance loads across a fixed reactance [2].

The beginning of the computer industry in the 1950's led to the advancement in modeling and analysis of detailed systems. The increasing complexity of the network from this point on has led a primary focus of electrical networks toward transient stability. The primary tool for stability analysis has therefore become the transient stability program. These programs, however, are only as good as the models and data supplied to them.

Present trends in the planning and operation of power systems have led to new kinds of stability problems. These problems are also fueled by the uncertainty in system components. Composition and characteristics of the load is one area that has contributed to the significant changes occurring in the dynamics of the overall power system. These changes have become more common and therefore a greater concern for transient stability than previously realized [2].

2.1 TRADITIONAL LINEAR LOAD MODELS

Generation, transmission, and distribution are essential components to the overall power system model. The research and understanding of the static and dynamic behavior of source-side components have led to their detailed models. The static and dynamic behavior of the composite load, however, has typically been harder to depict.

Modeling system load is complicated because the load is composed of millions of individual components connected to the system at any instance in time. These loads continuously change due to the time of day, weather, and state of the economy. There is also much uncertainty on how individual loads react differently to small and large voltage and frequency variations. It is impractical to represent all loads in a stability study, a fact that has led to the development of simplified composite load models [4].

Load models are typically located in stability studies at the network bus and are represented as an average power. These models therefore include all components down-line from the substation which can be seen in Figure 2.1 looking from bus A toward the individual feeders. These components include transformers, power lines, shunt capacitors, and voltage regulators in addition to the end-user load.

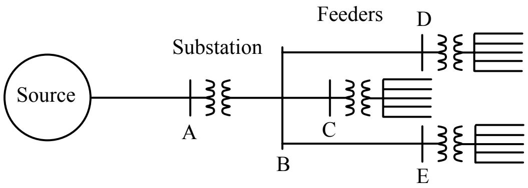


Figure 2.1. Radial system one-line diagram.

Static and dynamic load models are two types of load models most often used in stability studies. Static models represent system active and reactive load as an algebraic function of voltage and frequency. These models are best suited for loads where the steady state response to change in voltage and frequency is reached quickly. Dynamic loads models, represented with differential equations, take into account the past and present values of voltage and frequency. Dynamic loads typically take longer to reach steady state than static loads; however, they are commonly represented with the static load models [4].

2.1.1 Static Models

The three generic static load models are constant impedance, constant current, and constant power. In the constant impedance model, the load power varies with the square of voltage. In the constant current model, the load power varies in proportion with voltage. The load power, in the constant power model, does not change with voltage. These responses are typical for small perturbations in voltage but may not accurately reflect the response due to larger voltage sags. Voltage sags greater than 20% can cause sensitive loads to trip off-line. These models, however, have been accepted in practice and are used in many transient stability programs [4].

2.1.1.1 Exponential Model

The most common and widely practiced static load model is the exponential load model derived in [2]. The static exponential model depicts the change in active power P and reactive power Q as an algebraic function of voltage and frequency. The active and reactive exponential models are described by

$$P = P_0 \cdot \left[\frac{V}{V_0}\right]^{\left(dP/dV\right)} \cdot \left[1 + K_{pf} \cdot \left(f - f_0\right)\right], \tag{2-1}$$

$$Q = Q_0 \cdot \left[\frac{V}{V_0}\right]^{\left(dQ/dV\right)} \cdot \left[1 + K_{qf} \cdot \left(f - f_0\right)\right], \tag{2-2}$$

where P_0 ans Q_0 are the total active and reactive load, respectively; K_{pf} and K_{qf} are the active and reactive load frequency characteristics; (f–f_0) is the deviation in system frequency; dP/dV and dQ/dV are the active and reactive load power characteristics, respectively; and V and V_0 are the actual and nominal RMS voltages, respectively. Since the system frequency is not an inherent variable in most stability programs, the response due to frequency is typically neglected. The active and reactive exponential load models defined in (2-1) and (2-2), respectively reduce to

$$P = P_0 \cdot \left[\frac{V}{V_0}\right]^{\left(dP/dV\right)} \tag{2-3}$$

$$Q = Q_0 \cdot \left[\frac{V}{V_0}\right]^{\left(dQ/dV\right)} . \tag{2-4}$$

The exponential load model depicts the actual current response seen in Figure 2.2 for a linear load subjected to a five cycle 25% voltage sag.

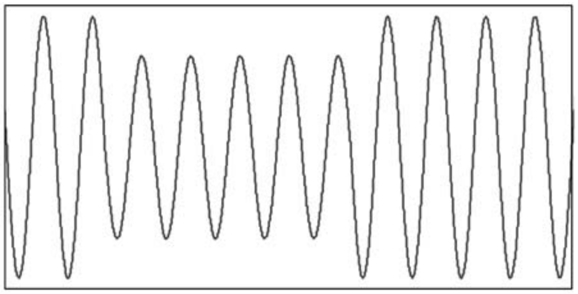


Figure 2.2. Linear load current response for a simulated five cycle voltage sag.

Constant power, current, and impedance loads have characteristics equal to 0, 1, and 2, respectively. For composite system load, the exponential model active power characteristic typically ranges from 0.5 to 1.8, and the reactive power characteristic typically ranges from 1.5 to 6. Due to magnetic saturation in transformers and motors, the reactive load is significantly higher than constant impedance. The most commonly accepted linear load model characteristics are constant current for active load and constant impedance for reactive load [2].

2.1.1.2 Polynomial Model

Another common static load model is the polynomial load model which is also referred as the ZIP model. This model represents the composite load as a combination of constant impedance, constant current, and constant power loads. The load power varies with the change in system voltage. The polynomial model is defined as

$$P = p_1 \cdot \left(\frac{V}{V_0}\right)^2 + p_2 \cdot \left(\frac{V}{V_0}\right)^1 + p_3 , \tag{2-5}$$

$$Q = q_1 \cdot \left(\frac{V}{V_0}\right)^2 + q_2 \cdot \left(\frac{V}{V_0}\right)^1 + q_3 , \tag{2-6}$$

where p_1, p_2, and p_3 are the constant impedance, constant current, and constant active power load, respectively; and q_1, q_2, and q_3 are the constant impedance, constant current, and constant reactive power load, respectively.

2.1.1.3 EPRI Model

The Electric Power Research Institute (EPRI) developed its own static load model under several research projects starting in 1976. By 1987, the model had gone through many revisions and can be found in [5]. EPRI's model represents the active load with two components, the first frequency and voltage dependent and the second only dependent on voltage. The reactive load also has two components. The first is the total reactive load, and the second is the total reactive load minus shunt capacitance.

2.1.2 Dynamic Model

The most influential dynamic load on the system is the induction motor which typically consumes approximately 60-70% of the total power generated. When large amounts of these motors are concentrated in small areas, the dynamic load model is preferred over the static model [4].

The equivalent circuit for the induction motor can be seen in Figure 2.3. The circuit components include the stator impedance (R_s, L_s), rotor impedance (R_r, L_r), and magnetizing inductance (L_m). The dynamics of this load can be taken to different levels of detail depending on the modeling program. Mechanical, rotor flux, and stator flux dynamics are commonly modeled for induction motors [4].

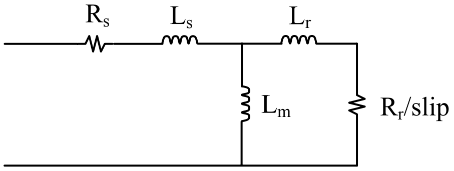


Figure 2.3. Induction motor equivalent circuit.

The dynamic load model is described in [6] by

$$\dot{x}(t) = -\frac{x(t)}{T_p} + P_o\left[\frac{V(t)}{V_o(t)}\right]^{N_{ps}} - P_o\left[\frac{V(t)}{V_o(t)}\right]^{N_{pt}}, \tag{2-7}$$

$$P_d(t) = \frac{x(t)}{T_p} + P_o\left[\frac{V(t)}{V_o(t)}\right]^{N_{pt}}, \tag{2-8}$$

$$\dot{z}(t) = -\frac{z(t)}{T_q} + Q_o\left[\frac{V(t)}{V_o(t)}\right]^{N_{qs}} - Q_o\left[\frac{V(t)}{V_o(t)}\right]^{N_{qt}}, \tag{2-9}$$

$$Q_d(t) = \frac{z(t)}{T_q} + Q_o\left[\frac{V(t)}{V_o(t)}\right]^{N_{qt}}, \tag{2-10}$$

where P_d and Q_d are the load active and reactive power demand, respectively; P_o, Q_o, and V_o are the nominal active power, reactive power, and voltage, respectively; T_d and T_q are the time constants for load state variables $x(t)$ and $z(t)$, respectively; and N_{ps}, N_{qs}, N_{pt}, and N_{qt} are the steady state and transient voltage load characteristics. The dynamic models (2-8) and (2-10) are equivalent to the exponential models (2-3) and (2-4) when $x(t) = 0$.

2.2 LINEAR LOAD MODEL IMPACT ON STABILITY

The type of loads and their location in the system has different impacts on stability. During a fault, if loads near accelerating machines are constant impedance, the generation-load power imbalance would be greater than if the loads had been constant power. Constant power loads near decelerating machines can further aggravate the system [4].

2.3 STATIC EXPONENTIAL LINEAR LOAD MODEL CHARACTERISTICS

The two primary techniques to determine the composite load model static characteristics are the measurement- and component-based procedures. The measurement-based procedure, developed and used in [6]-[11], determines static load characteristics using actual power flow data acquired at substations during voltage and frequency variations. The component-based procedure, developed by EPRI starting in 1976, categorizes the system load into load classes such as residential, commercial, and industrial [5].

Typical load class characteristics have been included in Table 2.1 from commonly cited references [12]. These classes are defined by their load components such as lighting, heating, air conditioning, and so on. Individual load component characteristics have been studied in detail, and several common appliance characteristics are included in Table 2.2 [2]. The EPRI program 'LOADSYN,' described in [5], converts the component characteristics into composite load characteristics to be used in transient stability programs.

A survey given to 85 industry representatives in 1988 concluded the majority of utilities were not using any methods to determine load model characteristics. The few that did were using the EPRI program 'LOADSYN'. Very few indicated any use of dynamic load modeling, and for the stability simulations where dynamic models would be most beneficial, static models were most commonly used. Most all indicated that they were dissatisfied with their present load models and were working to improve them [4].

Table 2.1. Load Class Characteristics for Aggregate Loads.

Load Class	Power Factor	*dP/dV*	*dQ/dV*	*Kpf*	*Kqf*
Residential					
Summer	0.9	1.2	2.9	0.8	-2.2
Winter	0.99	1.5	3.2	1	-1.5
Commercial					
Summer	0.85	0.99	3.5	1.2	-1.6
Winter	0.9	1.3	3.1	1.5	-1.1
Industrial	0.85	0.18	6	2.6	1.6

Table 2.2. Load Component Characteristics for Individual Loads.

Component	Power Factor	*dP/dV*	*dQ/dV*	*Kpf*	*Kqf*
Air conditioner					
3-phase central	0.9	0.088	2.5	0.98	-1.3
1-phase central	0.96	0.202	2.3	0.9	-2.7
window type	0.82	0.468	2.5	0.56	-2.8
Water Heater	1	2	0	0	0
Oven, Range top					
Deep fryer					
Dishwasher	0.99	1.8	3.6	0	-1.4
Clothes washer	0.65	0.08	1.6	3	1.8
Clothes dryer	0.99	2	3.2	0	-2.5
Refrigerator	0.8	0.77	2.5	0.53	-1.5
Television	0.8	2	5.1	0	-4.5
Incandescent lights	1	1.55	0	0	0
Fluorescent lights	0.9	0.96	7.4	1	-2.8
Industrial motors	0.88	0.07	0.5	2.5	1.2
Fan motors	0.87	0.08	1.6	2.9	1.7
Agricultural pumps	0.85	1.4	1.4	5	4
Arc furnace	0.7	2.3	1.6	-1	-1
Transformer (unloaded)	0.64	3.4	11.5	0	-11.8

Chapter 3 – Using Transmission Voltage Sag Data to Determine the Fraction of Distribution Feeder Load Due to Single-Phase Power Electronics

This chapter describes a new method to determine the composition of distribution feeder load by using data readily available from substation relays, captured when transmission voltage sags occur. Feeder current is decomposed into two components, linear and power electronic, by analyzing voltages and currents prior to and during voltage sags. The method is tested using 122 actual utility feeder events and is backed up by laboratory tests. For the 122 events, the power electronic load percentage of total megawatt demand is in the range of 5-15%, depending on season.

In addition to determining the power electronic component, the procedure also evaluates the linear load modeling characteristics needed for conventional stability studies.

3.1 INTRODUCTION

We begin by observing actual load response data during a transmission sag that has been recorded by a substation power quality monitor on a 13kV residential distribution feeder in Austin, TX. In Figure 3.1, the normalized voltage (dashed line) and current (solid line) are shown for a five cycle, 15% voltage sag. The majority of the load current is 60Hz sinusoidal, but a fraction of the load is single-phase power electronic which causes the triangular peaked current distortion due to capacitor filtered diode bridge AC/DC rectification.

The transient response of the power electronic load is quite different than traditional linear load. Using the decomposition technique developed in this chapter, the power electronic load current component from Figure 3.1 is calculated, and the estimated response of that load to the sag is shown in Figure 3.2. As can be seen, the composite power electronic load momentarily disconnects from the system, while its ride-through power is provided by the DC capacitors of the bridge rectifiers. During the sag, the DC capacitor voltage slowly decays to a new steady state. As the voltage decays, load slowly begins to reconnect to the system. At voltage sag recovery, the load then requires substantial power to recharge the capacitors to their original steady state voltage.

As we will show later, the percentage of power electronic load in Austin can reach as high as 15% of the total residential MW demand in the winter and can be as low as 5% in the summer. The overall MW demand of the power electronic load, however, is relatively constant throughout the year.

Concerning stability load models, previous measurement-based procedures for calculating modeling characteristics [1]-[6] do not distinguish between linear and power electronic load. And yet, the responses of the two types of loads to voltage sags are considerably different. This chapter determines the linear load characteristics needed for the traditional exponential linear load model (represented by (2-3) and (2-4)) by decomposing the composite load into linear and nonlinear components and then observing the variation of linear load with sag voltage.

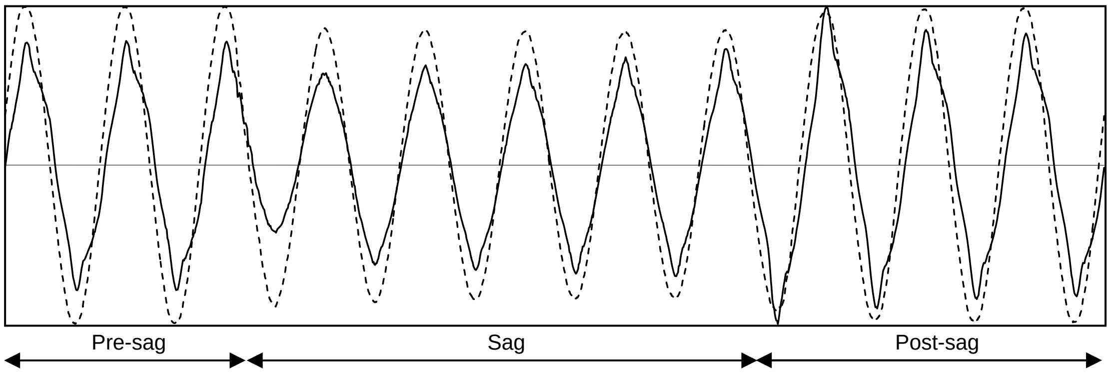


Figure 3.1. Utility voltage sag and current response on 13kV distribution feeder (Solid line is current, dashed line is voltage).

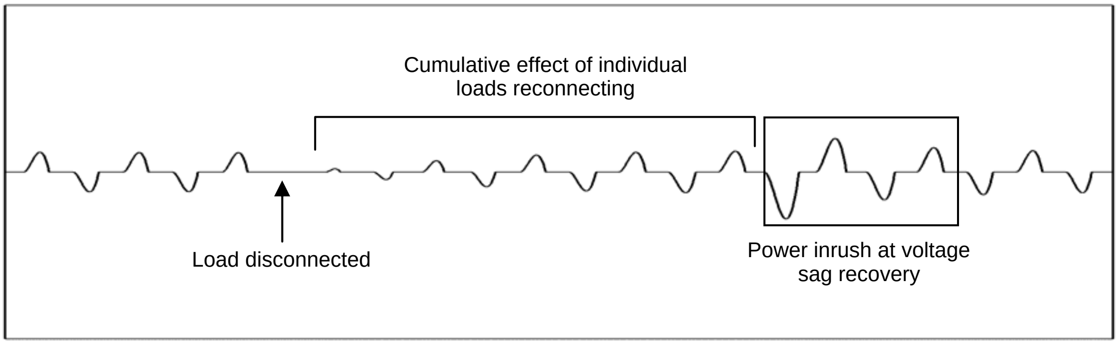


Figure 3.2. Estimated utility power electronic load current response for event in Figure 3.1 (same scale).

3.2 ILLUSTRATION OF THE MEASUREMENT-BASED PROCEDURE USING LABORATORY VOLTAGE SAG TESTS

3.2.1 Voltage Sag-Test Station

The laboratory Voltage Sag-Test Station, developed in [1], is used to generate the load response for which the measurement-based procedure is applied. A block diagram of the station can be seen in Figure 3.3.

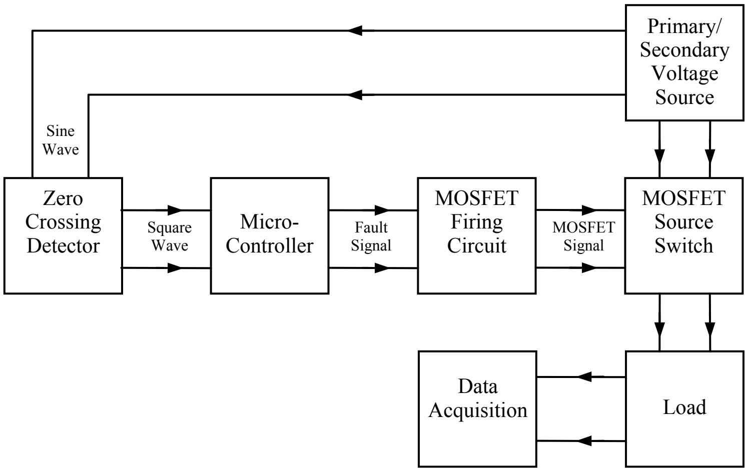
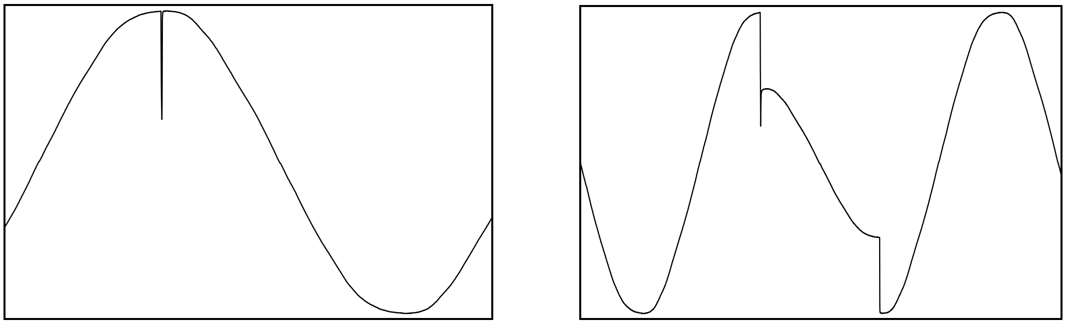
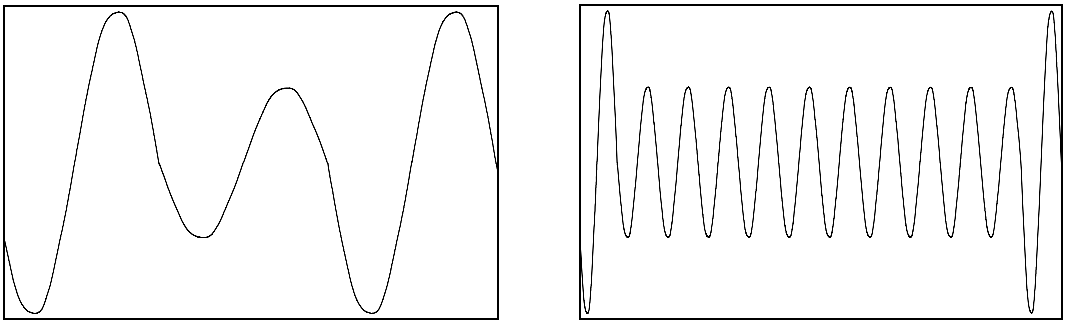


Figure 3.3. Voltage Sag-Test Station hardware block diagram.

Timed by the zero crossing of the voltage sine wave, a fault trigger signal is generated with the microcontroller accurate to within one degree of a 60 Hz cycle. The trigger signal is then sent from the microcontroller to the hardware to create the simulated sag. This is done when the optically isolated MOSFET firing circuit inputs the trigger signal and sends out isolated switching signals to the MOSFETs. These signals control the MOSFETs which switch the load from the primary (constant) to secondary (variable) voltage source. Switching sources without discontinuity resembles actual voltage sags on upstream or parallel feeders. Four examples of 50% voltage sags for various starting degrees and durations are illustrated in Figure 3.4.



(a) 90 degree start, one degree sag (b) 90 degree start, half cycle sag



(c) 180 degree start, one cycle sag (d) 180 degree start, ten cycle sag

Figure 3.4. Various voltage sags created by the Voltage Sag-Test Station.

3.2.2 Properties of Linear and Single-Phase Power Electronic Load

Unique waveform properties of linear and power electronic load allow one to identify and decompose the composite load. Linear load is predominately harmonic-free as long as the voltage harmonic distortion is low, and single-phase power electronic load has the distinct property in which current is drawn from the system for only a short interval twice every power frequency cycle. This short period of current occurs in-phase and near the peak of the voltage waveform causing the load to be primarily active power. For the rest of the cycle, the system power electronic load current is zero. Knowing these unique properties, one can perform a curve fitting routine to determine the linear and nonlinear load.

3.2.3 Decomposition of Fan Plus Computer Monitor Load

The waveform in Figure 3.5 shows the actual response of a fan plus computer monitor when subjected to a 25% laboratory generated voltage sag. The power electronic load causes the triangular peaks seen in the current waveform. One power frequency cycle of current during pre-fault (boxed region in Figure 3.5) is illustrated in detail with curve (a) in Figure 3.6.

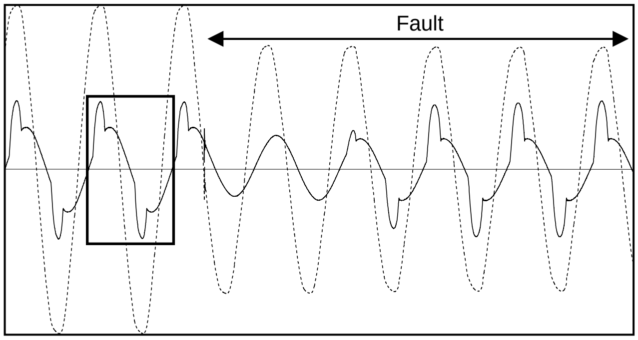


Figure 3.5. Actual response of fan plus computer monitor (Dashed line is voltage, solid line is current).

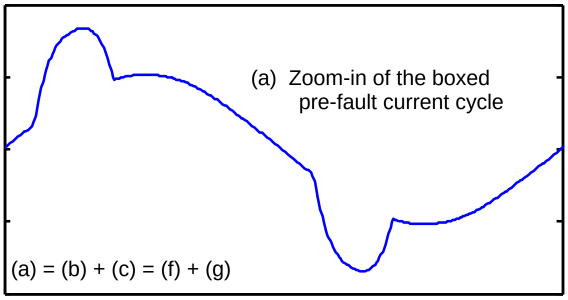


Figure 3.6. Zoom-in of pre-fault current cycle from Figure 3.5.

The decomposition process begins with an FFT of curve (a). The resulting fundamental component is illustrated with curve (b) in Figure 3.7.

Assuming the linear load is harmonic free, then all current harmonics above the fundamental are due to the nonlinear load. Therefore, using the distortion harmonics above the fundamental, the nonlinear load less its fundamental component is

$$I_D = \sum_{n=2}^{\infty} I_n \cdot \cos\left(2\pi fn \cdot t + \theta_n\right). \tag{3-1}$$

and shown with curve (c) in Figure 3.7. Curve (c) = curve (a) – curve (b).

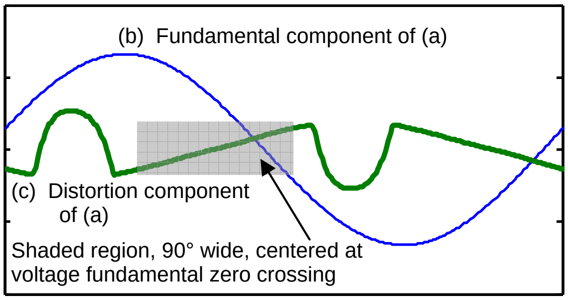


Figure 3.7. FFT fundamental and distortion waveform from Figure 3.6.

Because the dominant nonlinear load in our feeder is single-phase power electronic, we are able to determine the fundamental component of the nonlinear load by using a least squares approximation to fit the shaded region of curve (c). Since the power electronic load current during that time period is actually zero, we can say that the fundamental component of the nonlinear load is the negative of the fundamental curve fit of the shaded region. The fundamental curve fit is shown as curve (d) in Figure 3.8, and the negative of curve (d) is curve (e).

The nonlinear load fundamental component amplitude I_{NL} and phase θ_{NL} can be determined from the shaded region of curve (c) with the following four equations:

$$I_{NL} \cos\left(\omega \cdot t + \theta_{NL}\right) = -I_D \tag{3-2}$$

$$\begin{bmatrix} \cos(\omega \cdot t) & -\sin(\omega \cdot t) \end{bmatrix} \cdot \begin{bmatrix} A \\ B \end{bmatrix} = -I_D \tag{3-3}$$

$$\theta_{NL} = \operatorname{atan} 2(B, A) \tag{3-4}$$

$$I_{NL} = \frac{A}{\cos\left(\theta_{NL}\right)} \tag{3-5}$$

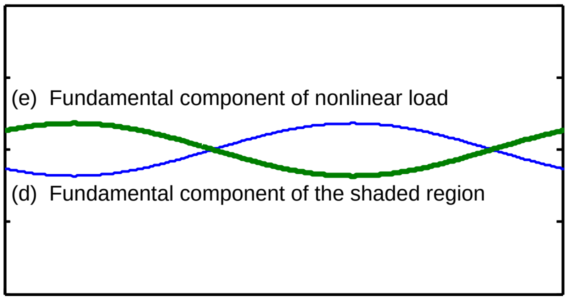


Figure 3.8. Distortion and nonlinear load fundamental component.

After solving the nonlinear fundamental amplitude I_{NL} and phase θ_{NL} the linear load amplitude and phase are determined by the sum of the fundamental sinusoids:

$$I_T \cdot \cos(\omega \cdot t + \theta_T) = I_L \cdot \cos(\omega \cdot t + \theta_L) + I_{NL} \cdot \cos(\omega \cdot t + \theta_{NL}) \tag{3-6}$$

where I_T and θ_T are the total FFT fundamental amplitude and phase, respectively; I_L and θ_L are the amplitude and phase of the linear load, respectively; and ω is 2πf. The amplitude and phase of the linear component are equal to

$$I_L = \sqrt{(I_T - I_{NL} \cdot \cos(\theta_{NL} - \theta_T))^2 + (I_{NL} \cdot \sin(\theta_{NL} - \theta_T))^2} \tag{3-7}$$

$$\theta_L = \tan^{-1}\left(- \frac{(I_{NL} \cdot \sin(\beta))}{(I_T - I_{NL} \cdot \cos(\beta))} \right) + \theta_T \, . \tag{3-8}$$

The actual linear and power electronic load currents are plotted in Figure 3.9 as curves (f) and (g), respectively. Linear load curve (f) = curve (b) – curve (e), nonlinear load curve (g) = curve (c) + curve (e), and total load curve (a) = curve (f) + curve (g). The linear load voltage and current phasors are used to determine the linear load active and reactive powers.

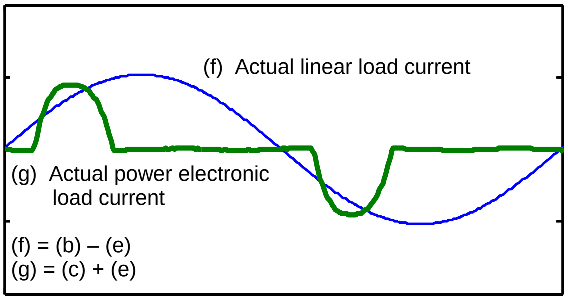


Figure 3.9. Decomposed fan plus computer monitor current.

3.2.4 Determination of Linear Load Characteristics

Having identified the linear and power electronic currents, we now determine the stability load modeling characteristics for the linear load. In [10], it is suggested that five cycles of sag are needed for the load to reach steady state. Our field measurements show that the linear load steady state is reached as quickly as 1-2 cycles, whereas the power electronic load takes longer. Because of the difference in the two response times, we can apply our linear load steady state analysis soon after the onset of the sag.

The decomposition procedure is repeated during the linear load steady state region of the sag to determine the sag linear active and reactive powers. Equations (2-3) and (2.4) are then used to determine the linear load characteristics *dP/dV* and *dQ/dV* by comparing the changes in *P* and *Q* from pre-sag to sag as

$$dP/dV = \frac{\ln(P_{fault}/P_{prefault})}{\ln(V_{fault}/V_{prefault})} \qquad (3\text{-}9)$$

$$dQ/dV = \frac{\ln(Q_{fault}/Q_{prefault})}{\ln(V_{fault}/V_{prefault})} \qquad (3\text{-}10)$$

3.2.5 Laboratory Linear Load Characteristics

In laboratory tests, we subject three common household loads (an incandescent light bulb, box fan, and a desktop computer monitor) to voltage sags. The experimentally determined linear load characteristics for the individual and combinations of composite loads are given in Table 3.1.

Table 3.1 Measured Individual and Composite Linear Load Characteristics.

	dP/dV	*dQ/dV*
Bulb (195W)	1.63	0
Box Fan (145W, 148VAR)	2.00	2.04
Monitor (75W)	0	0
Bulb, Box Fan	1.82	2.04
Bulb, Monitor	1.68	0
Box Fan, Monitor	2.02	2.05
Bulb, Box Fan, Monitor	1.79	2.05

The incandescent light bulb is a linear load that has an active power characteristic of 1.63 and a reactive power characteristic of zero which corresponds favorably to values recommended in Table 2.2. The box fan is a small induction motor with an active and reactive power component and characteristic. The monitor is a totally nonlinear power electronic load that has no linear load characteristics. When the composite load includes the monitor, the load characteristics are the same as those for the linear load. This verifies the ability of the decomposition procedure to successfully decompose the total load into its linear and nonlinear components.

3.3 UTILITY LOAD DECOMPOSITION

Utility feeder data captured by substation relays or power quality monitors can be decomposed into linear and nonlinear load components similar to that done for the laboratory load. Using the actual feeder data from Figure 3.1, the decomposition process is illustrated in Figure 3.10 for one cycle prior to the voltage sag. The decomposed linear and nonlinear load currents are shown by curves (f) and (g), respectively.

The composite load on the utility distribution feeder includes additional nonlinear loads other than power electronics, in particular, transformer magnetizing current. The nonlinear portion of the magnetizing current can be seen in curve (g) as the smaller pulse (M) following the power electronic load pulse (PE). The nonlinear portion of the magnetizing current poses no particular problem because

- there is little real power associated with (M),
- (M) is usually zero during the sag, and
- (M) has little impact on the fundamental component calculated in the shaded region of Figure 3.10.

For this particular feeder and event occurring in late November, the percent of pre-fault power electronic load is 10% of the total MW demand. Using 3.2.4, the linear load characteristics are determined using waveforms prior to and during the voltage sag. The computed values are $dP/dV = 1.45$ and $dQ/dV = 5.90$.

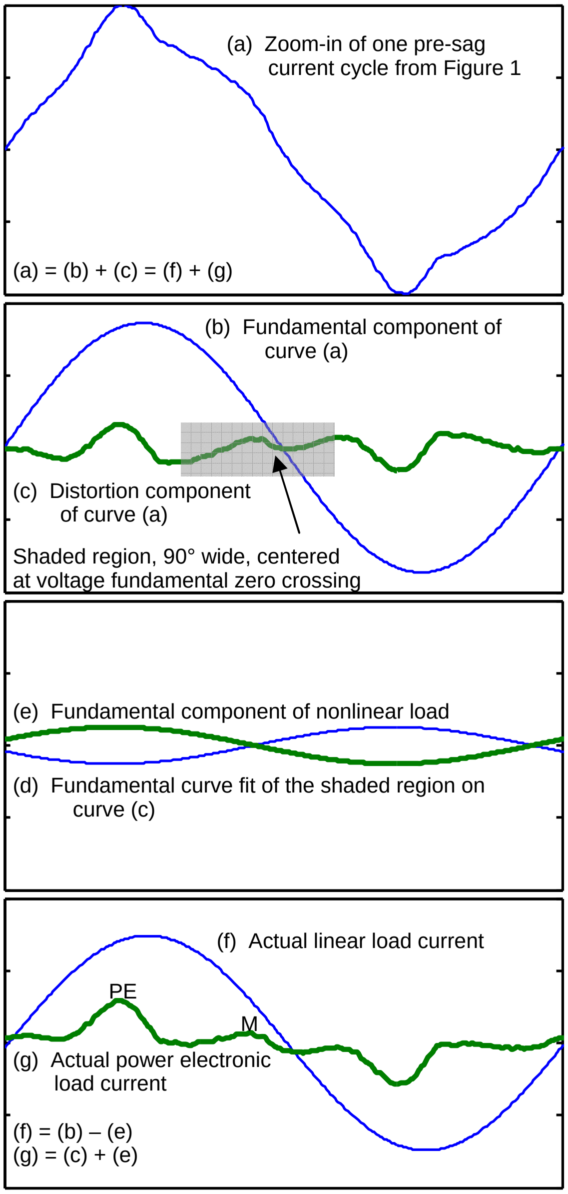


Figure 3.10. Decomposition of utility load current using pre-sag cycle of event in Figure 3.1.

3.3.1 Detailed Examination of Three Events and Comparison to ATP-EMTP Model Response

The utility linear load has been characterized for three 12% lightning-induced voltage sags. The determined linear active and reactive power characteristics are given in Table 3.2. Because these events are line-ground faults on the transmission system (high side of delta-wye step-down transformer), the third phase, Phase B, is unaffected and has therefore been left out of the table.

Table 3.2. Measured Utility Linear Load Characteristics.

	Phase A			Phase C		
Event	*dP/dV*	*dQ/dV*	% PE	*dP/dV*	*dQ/dV*	% PE
(a) 3/25/2005, 22:35:54	1.52	5.65	8.4	1.33	5.35	7.7
(b) 3/25/2005, 22:35:57	1.51	7.81	8.5	1.33	7.07	7.6
(c) 3/26/2005, 00:20:33	1.63	6.19	9.9	1.38	5.37	8.2

Characteristic *dP/dV* is similar in Events (a) and (b) for each phase. These events occur only three seconds apart, in which time, the composite linear and power electronic load did not change significantly. Characteristic *dP/dV* in Event (c), however, increases slightly from Events (a) and (b). Thus, the composition of linear load became closer to constant impedance and the percentage of power electronic load increased over the two-hour interval. The average Phase A *dP/dV* is slightly more constant impedance than constant current. The average Phase C *dP/dV* is slightly more constant current than constant impedance. These values compare favorably to those recommended in Table 2.1.

The reactive power load varies more with voltage than if it were constant impedance; therefore, the majority of reactive loads are operating in saturation prior to the voltage sag.

Characteristic *dP/dV* and *dQ/dV* have been validated by simulations performed in ATP-EMTP comparing the actual and simulated load response. The comparison of Phase C during Event (b) and can be seen in Figure 3.11. The actual and simulated current waveforms are identical before the fault indicating the correct amount of linear and power electronic load. When the fault occurs, there is a transient shift in the actual data that is not captured by the simulated model. After the first cycle in the fault, the linear load waveforms have a similar response. It is evident in the actual response that the power electronic load begins to come online, however, the simulated power electronic component is modeled ‘off’ at this time.

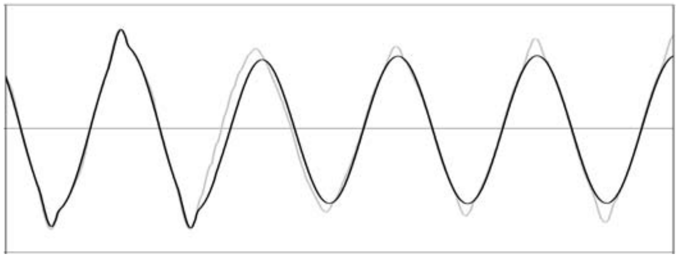


Figure 3.11. Actual (gray line) and simulated (black line) linear load current response.

3.3.2 Fraction of Power Electronic Load for the 122 Events

We determined the total amount of nonlinear power electronic load for each of the 122 events captured over a two year period on the distribution feeder. Each studied event is for the most affected phase. The monthly average single-phase power electronic MW demand per phase is shown in Figure 3.12. As expected, it is rather constant throughout the year.

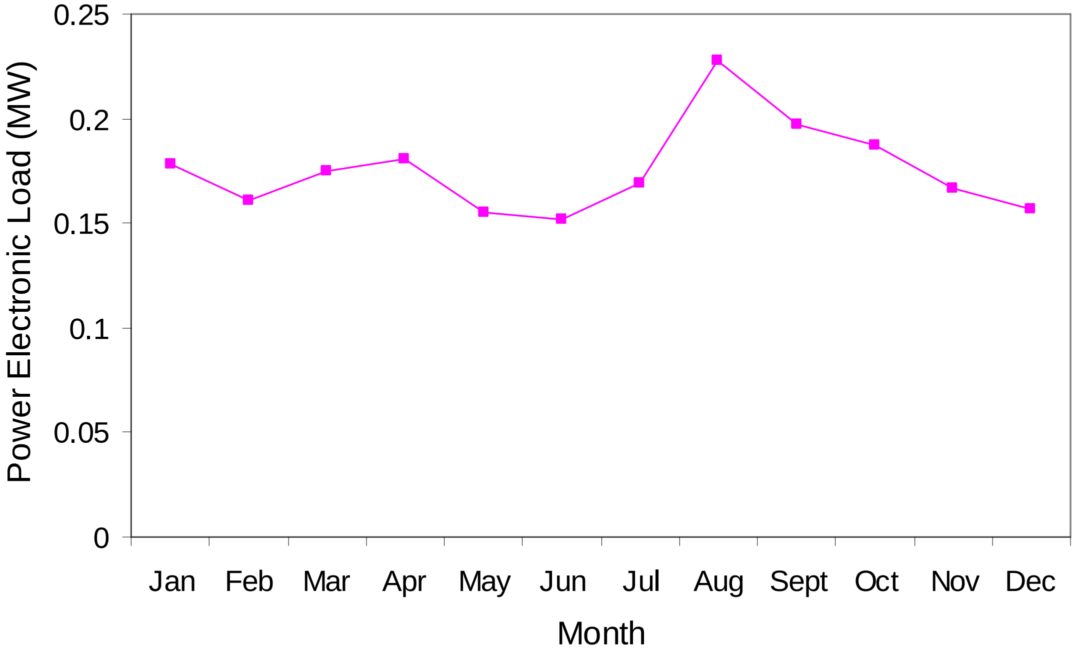


Figure 3.12. Monthly average power electronic load on the feeder, per phase.

Because the linear load varies by season, the percent of power electronic load changes by season. Figure 3.13 shows the monthly average power electronic load in percent of total feeder MW. In February, there is an increase in linear load, most likely due to electrical heating, which causes the percentage to decrease during this month. Due to air conditioning load, the percentage also greatly decreases in the summer.

The average fraction is greatest (12%) in December where there is little air conditioning or heating load. In the summer, the linear load approximately doubles due to air conditioning, which causes the power electronic percentage to decrease by approximately half. For example, the average percentage is 6% in August. For individual events, the seasonal percentage range is 5-15%.

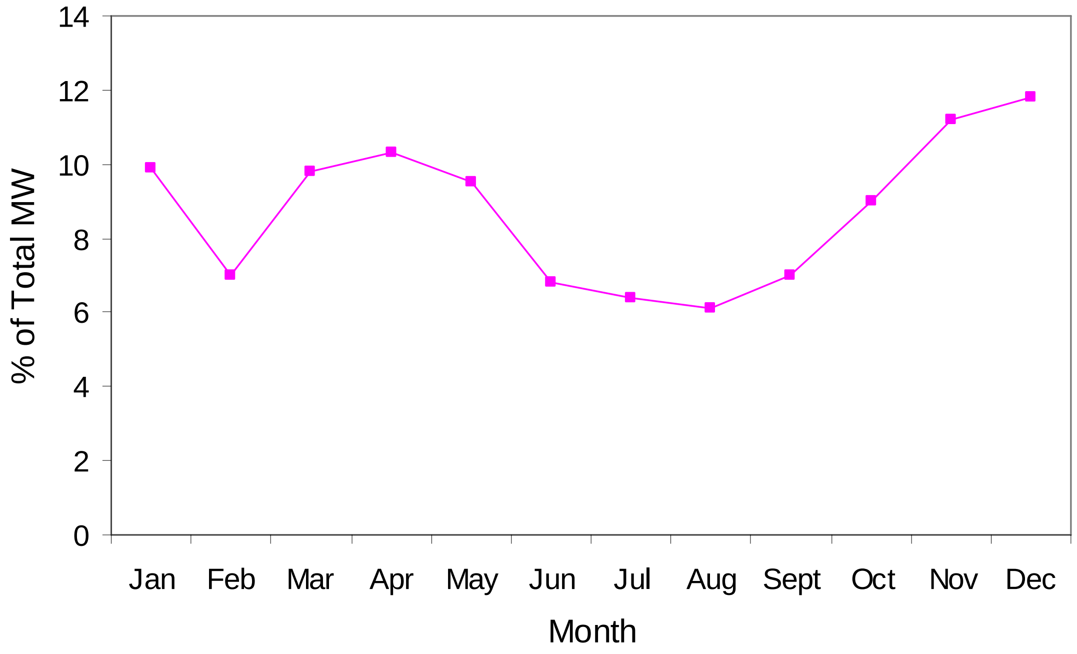


Figure 3.13. Monthly average power electronic load in percent of total feeder MW.

3.3.3 Seasonal Variation of Linear Load Modeling Characteristics

Characteristics *dP/dV* and *dQ/dV* are determined for the 84 events (of the total 122) that occurred strictly in the summer or winter months. Linear load characteristics for the summer months of June, July, and August are plotted in Figure 3.14. Recall that *dP/dV* = 1.0 is constant current and *dP/dV* = 2.0 is constant impedance. During these summer months, *dP/dV* averages 1.15 and *dQ/dV* averages 6.12. The linear active power load is primarily constant current, and the reactive load is much more voltage dependent than constant impedance.

Figure 3.15 shows the results for the winter months of December, January, and February. Characteristic *dP/dV* averages 1.62 and *dQ/dV* averages 5.45. The winter active power linear load is therefore slightly closer to constant impedance than constant current. Characteristic *dQ/dV* is still very large.

These average residential active power characteristics compare favorably to those suggested in Table 2.1 (i.e., 1.2 in summer and 1.5 in winter).

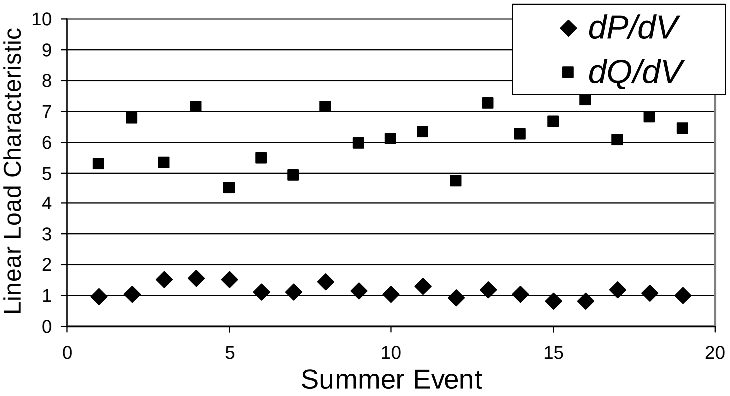


Figure 3.14. Summer linear load characteristics (*dP/dV* avg. = 1.15, *dQ/dV* avg. = 6.12).

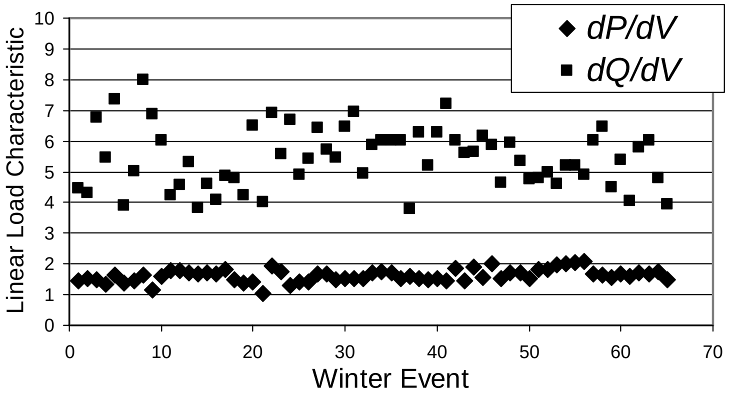


Figure 3.15. Winter linear load characteristics (*dP/dV* avg. = 1.62, *dQ/dV* avg. = 5.45).

3.4 SUMMARY

The measurement-based procedure described in this paper allows one to accurately decompose the composite load on a utility feeder into linear and single-phase power electronic components using readily available data captured by power quality monitors and feeder protection relays during transmission voltage sags. For our 122 tests, the power electronic load (in MW) on the residential feeder is shown to be relatively constant throughout the year. Expressed as a percent of total MW, it ranges from about 5% in the summer to 15% in the winter.

The transient response of power electronic loads is considerably different from linear loads. Power electronic loads have a constant power steady state characteristic; however, the dynamic behavior of these loads is not captured by the exponential load model. The linear load reaches steady state earlier than the power electronic load. Therefore, three-cycle events are typically long enough to provide the needed window of opportunity to compute linear load characteristics once the power electronic component has been identified and deducted.

The voltage response of the linear load is used to calculate the exponential load model characteristics *dP/dV* and *dQ/dV* required by most stability programs. The active power characteristics are strongly influenced by season. For the 19 summer events shown in Figure 3.14, the average load modeling characteristics are

- *dP/dV* = 1.15
- *dQ/dV* = 6.12.

For the 65 winter events shown in Figure 3.15, the average load modeling characteristics are

- *dP/dV* = 1.62
- *dQ/dV* = 5.45.

The active power characteristics for our 84 events are strongly influenced by season, varying from near constant current in the summer to near constant impedance in the winter. These observations compare favorably to commonly cited references.

Summarizing, the techniques described in this chapter allow electric utilities to use actual data to

1. estimate the percentage of single-phase power electronic load, and
2. automate the process of determining the appropriate stability models for linear loads.

Thus eliminates uncertainties in the load model. The power electronic transient load model is investigated further in the following chapters.

Chapter 4 – Harmonics

Nonlinear power electronic loads are rich in current harmonic distortion. The harmonic content, however, is dependent on the load voltage waveform. This chapter examines the impact that voltage distortion has on the current distortion of eleven common 120V single-phase loads. The study is conducted with a specially developed harmonics testing station in which feedback is applied to drive the load voltage to the desired target waveform. The results of 550 individual tests show that depending on load type, current distortion can vary dramatically with voltage distortion and depends on the individual voltage harmonic magnitudes and phase angles.

This chapter then illustrates the problems associated with using Norton equivalent models to represent single-phase nonlinear loads such as power electronics. Various voltage waveshapes with 5% THDv are applied to several types of single-phase nonlinear loads which allow one to compute the Norton parameters. The test results show that the Norton equivalent model for a nonlinear load is not unique and varies significantly with applied voltage waveshape.

4.1 EXPERIMENTAL APPARATUS, TESTING RESULTS, AND INTERPRETATION OF THE IMPACT OF VOLTAGE DISTORTION ON THE CURRENT DISTORTION OF TYPICAL SINGLE-PHASE LOADS

4.1.1 Introduction

Current distortion (THDi) tests for individual appliances are supposed to be made using a low-distortion voltage (i.e., near-perfect sinewave) [13]. In practice, it is difficult to obtain a near-perfect sinusoidal voltage in any commercial building because of harmonic pollution in the building. Even if an amplifier is used, load currents interacting with the amplifier impedance corrupts the voltage waveform. As a result, actual test voltage waveforms can have 2-4% total harmonic voltage distortion (THDv), and the individual harmonics are uncontrollable and can vary considerably.

Technical literature is rich with publications [14-16] that document the effect that THDi has on THDv. However, there are very few references available about the reverse effect – i.e., what impact does THDv have on THDi [17]?

This section illustrates the effect of THDv on THDi through 550 carefully controlled tests, where a harmonics testing station with corrective feedback on the load voltage energizes 120V, single-phase loads with precision voltage waveforms. The results illustrate the sensitivity of common single-phase loads to voltage harmonics. Sensitivity varies considerably with load type.

4.1.2 Harmonic Testing Station

4.1.2.1 Station Design

The harmonics testing station, developed for CenterPoint Energy, uses an inverter together with software written in LabVIEW [18], to create a single-phase 120Vrms, 50/60Hz AC voltage with a desired harmonic spectral content (through the 25th harmonic) for loads up to 1.5kW. The two unique features of the station are the following:

- The testing station compensates for the distorting impact that harmonic currents in the test load have on the applied voltage by employing a specially-developed feedback method to adjust the load voltage spectrum to the desired target. The station minimizes the total individual harmonic voltage error, normalized to the fundamental, within 1%.
- The testing station has the ability to operate in either a 'stand alone' mode where it provides all the load power, or in a 'summing junction' mode where it synchronizes with the grid and adds to the building voltage. Thus, the testing station need only provide the harmonic portion of the desired load voltage plus a few percent of the harmonic load power.

Illustrations for the ‘stand alone’ and ‘summing junction’ operating modes are given in Figure 4.1 and 4.2, respectively. The inverter shown was specifically built for the harmonic testing station. The inverter operates at 150kHz, takes power from a 250Vdc bus, and is rated 1.5kW.

In the stand alone mode, the inverter provides all the load voltage to power the test load. This configuration limits the size of the test load to the rated limit of the inverter. The advantage of this mode is that the base frequency is constant for all harmonics throughout the test.

In the summing junction mode, the inverter supplies only the harmonic voltage and power needed to achieve the desired load voltage waveform. This increases the effective power rating of the testing station by an order of magnitude. The summing junction operating mode also has the unique ability to correct the building voltage to a near perfect sinewave or other desired waveshape for testing purposes.

The disadvantage of the summing junction mode is that as the system frequency changes, the proper summing of the system voltage and harmonics may become slightly out of phase. Thus, constant synchronization with the grid frequency must be performed. When the grid frequency is changing steadily, the station has no problem staying synchronized with the system. An extreme change in frequency, such as the loss of a large generator, causes a loss of synchronism momentarily.

To maintain synchronism, the point-by-point station output voltage for several cycles is determined to match the grid frequency and placed into a buffer. The buffer is then aligned to play out from a system zero crossing, and each time the buffer is updated with new points, it replaces the old points and concatenates at a zero crossing.

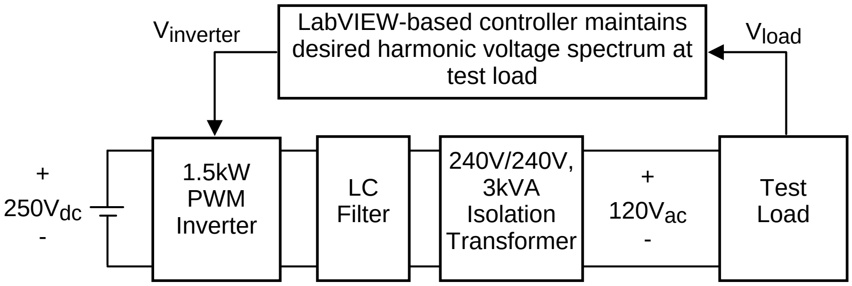


Figure 4.1. Stand alone operating mode with harmonic-controlled V_{load} (inverter supplies all load voltage and power to the test load).

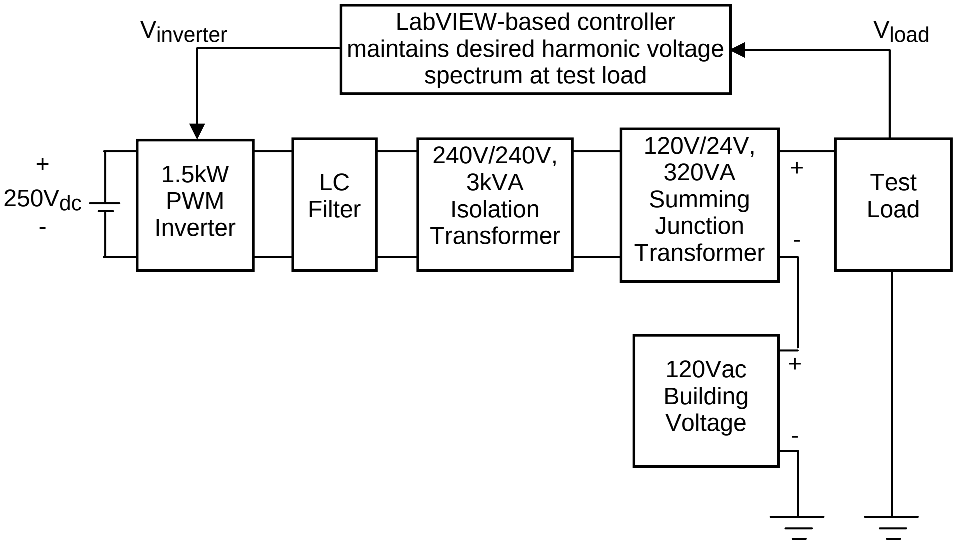


Figure 4.2. Summing junction operating mode with harmonic-controlled V_{load} (inverter adds or corrects voltage distortion to the building voltage and supplies only the required harmonic voltages and harmonic power to the test load).

4.1.2.2 Feedback Routine

All amplifiers and inverters have output impedances. Thus, when powering a nonlinear load, harmonics in the load current create undesired harmonics in the amplifier/inverter output voltage. Feedback is necessary to adjust the amplifier/inverter input voltage in such a way that the output voltage waveform is driven to the desired target.

Consider the feedback loop in the stand alone mode in Figure 4.1. Inverter input signal $V_{inverter}$ is comprised of two components – the user specified target value V_{target}, plus the computed correction needed (i.e., $V_{feedback}$) to drive the load voltage to the target value. Thus,

$$V_{inverter} = V_{target} + V_{feedback} , \tag{4-1}$$

so that

$$V_{error} = V_{target} - V_{load} = 0 . \tag{4-2}$$

For the summing junction mode in Figure 4.2, $V_{inverter}$ does not contain the portion of V_{target} that is supplied by the 120Vac building voltage. Thus,

$$V_{inverter} = V_{target} - V_{buildingvoltage} + V_{feedback} . \tag{4-3}$$

There are two methods for adjusting $V_{feedback}$ in the harmonics testing station, and each applies to both stand alone and summing junction operating modes. First, the user can make manual adjustments to the individual harmonic components of $V_{feedback}$ (i.e., the 'Manual Method'). The manual method is useful for making simple corrections and for illustrating the interaction between load current harmonics and inverter output voltage. However, it is usually impossible to manually reduce V_{error} to the 1% range, especially when testing nonlinear loads.

The second feedback adjustment procedure is automatic and iterative. This iterative procedure employs the method of finite differences, where small changes are made to the individual harmonic components of $V_{feedback}$ and the corresponding changes in like harmonics of V_{error} are observed. This does mean that the interaction between harmonics is ignored, however, for any iteration only the most offending harmonic is controlled.

Each iteration begins by identifying the harmonic k that has the highest V_{error} magnitude. Then, partial derivatives are approximated from finite differences, and $V_{feedback}$ is adjusted accordingly to reduce V_{error}.

Expressing harmonic k components of $V_{feedback}$ and V_{error} as phasors in rectangular form, we have

$$\tilde{V}_{feedback}^{k} = V_{f,real}^{k} + jV_{f,imag}^{k} \tag{4-4}$$

and

$$\tilde{V}_{error}^{k} = V_{e,real}^{k} + jV_{e,imag}^{k} \, . \tag{4-5}$$

The objective is to adjust $V_{f,real}^{k}$ and $V_{f,imag}^{k}$ so that $V_{e,real}^{k}$ and $V_{e,imag}^{k}$ approach zero. For small changes,

$$\begin{bmatrix} \Delta V_{e,real}^{k} \\ \Delta V_{e,imag}^{k} \end{bmatrix} = \begin{bmatrix} \dfrac{\partial V_{e,real}^{k}}{\partial V_{f,real}^{k}} & \dfrac{\partial V_{e,real}^{k}}{\partial V_{f,imag}^{k}} \\ \dfrac{\partial V_{e,imag}^{k}}{\partial V_{f,real}^{k}} & \dfrac{\partial V_{e,imag}^{k}}{\partial V_{f,imag}^{k}} \end{bmatrix} \begin{bmatrix} \Delta V_{f,real}^{k} \\ \Delta V_{f,imag}^{k} \end{bmatrix} . \tag{4-6}$$

At any iteration m, one must compute the changes in feedback voltage that will reduce the error to zero at iteration m+1. Writing (4-6) as

$$[\Delta V_e] = [J][\Delta V_f] \; , \tag{4-7}$$

then expanding (4-7) to

$$[V_e]_{m+1} - [V_e]_m = [J]_m \left\{ [V_f]_{m+1} - [V_f]_m \right\} , \tag{4-8}$$

and setting the $[V_e]_{m+1}$ term to the desired value (i.e., 0), yields

$$[V_f]_{m+1} = [V_f]_m - [J]_m^{-1} [V_e]_m \, . \tag{4-9}$$

Summarizing, the partial derivatives given in the above Jacobian matrix are evaluated using the method of finite differences, and then new values of feedback are computed for harmonic k.

4.1.3 Test Conditions

4.1.3.1 Loads

The eleven test loads are all relatively new and are representative of common loads found in residences or office buildings. Sorted by sinusoidal THDi, the loads are included in Table 4.1.

Table 4.1. Test Loads.

Load	THDi (%)	Power (W)
Incandescent lamp	1.0	213
Box fan	1.7	147
Refrigerator	6.1	175
T8 fluorescent lamp, electronic ballast	6.6	108
T12 fluorescent lamp, electronic ballast	13.3	152
T12 fluorescent lamp, magnetic ballast	16.9	190
Window air conditioner, compressor & fan	17.3	488
Microwave oven	38.6	1610
Window air conditioner, fan only	50.0	60
Compact fluorescent lamp (five bulbs)	107	68
Personal computer, without monitor	152	34

The first seven loads are low distorting with THDi less than 20%. The next two are moderate distorting loads with THDi between 20% and 60%. The last two are high distorting loads with THDi greater than 60%.

4.1.3.2 Voltage Waveforms

The test voltage waveforms have an underlying 120Vrms, 60Hz fundamental component. Harmonics through the 25th multiple can be added individually, or together, to add distortion. Even-ordered harmonics are zero in the test voltage because they are usually negligible in building supply voltages. With the use of feedback, the load voltage waveforms are controlled to within 1% of the desired target waveform. The waveforms are

3. Sinusoidal voltage
4. Simulated building voltage having THDv = 5% and a typical building voltage waveshape (Figure 4.3) and harmonic content (Table 4.2).
5. Sinusoidal voltage plus 5% or 10% single odd-harmonic voltage 3rd, 5th, … , 25th, and with harmonic phase angles either 0º, 90º, 180º, or 270º.

The 5% THDv simulated building voltage in Figure 4.3 is fairly typical in commercial buildings. The building voltage is flattened due to large numbers of computers and other single-phase power electronic loads that draw current for a short interval near the voltage peak. The waveform shown has a somewhat higher THDv than normally seen, but it is still within the limit of what is considered acceptable (i.e., 5%).

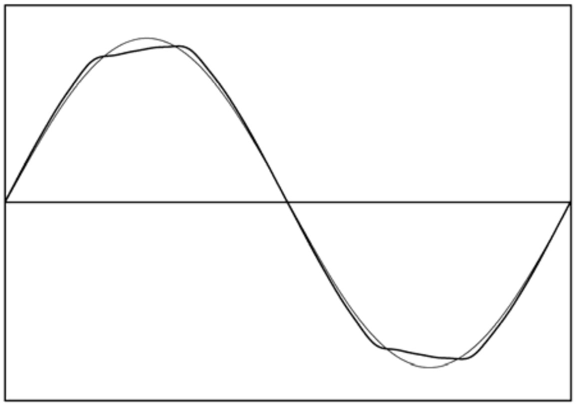
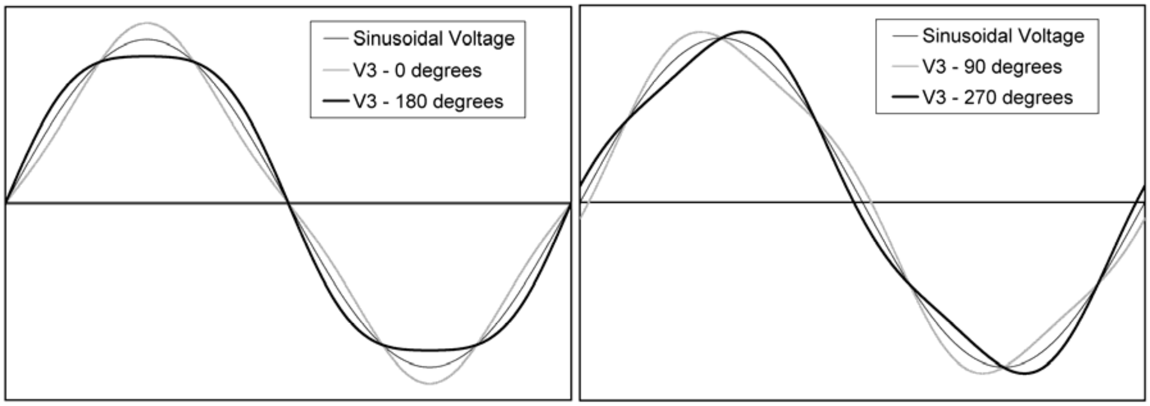


Figure 4.3. Sinusoidal and 5% THDv building voltage.

Table 4.2. 5% THDv Building Voltage Harmonic Magnitudes and Angles.

Harmonic	Magnitude – % of fundamental	Phase – sine reference
1	100	0
3	4.1	16
5	2.5	203
7	1.0	38
9	0.1	9
11	0.5	219
13	0.3	239
15	0	0
17	0.2	239
19	0.1	69

An example of the single harmonic distortion for the 3rd harmonic at 0º and 180º can be seen in Figure 4.4a. The 3rd harmonic at 90º and 270º is shown in Figure 4.4b. It is obvious in Figure 4.4 that harmonic magnitude alone does not well describe a waveshape, which can be peaky, flattened, skewed left, or skewed right. The voltage waveshape is very significant in determining the THDi of many loads.



(a) (b)

Figure 4.4. Sinusoidal and harmonic voltage with 10% 3rd harmonic (a) 0º and 180º phase shifts and (b) 90º and 270º phase shifts (cosine reference).

4.1.4 Test Results Using Simulated Building Voltage

Comparisons of load THDi for the sinusoidal and 5% THDv simulated building voltage are shown in Figure 4.5.

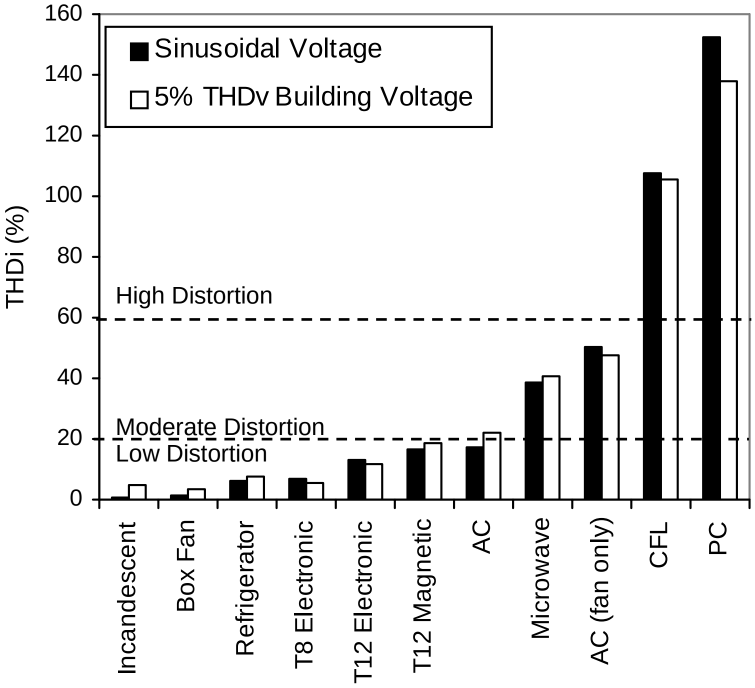


Figure 4.5. THDi for test loads excited by sinusoidal and 5% THDv building voltage. Three ranges are specified by low, moderate, and high distorting loads.

The simulated 5% THDv building voltage can produce either higher or lower THDi than sinusoidal voltage. Specifically, the electronic ballasts and the fan of the window air conditioner have lower THDi when energized by the simulated building voltage. Also, the simulated building voltage has the flattened shape that causes the high distorting loads to conduct for longer periods of time each half cycle, thus reducing their THDi. Table 4.3 lists the THDi response of the loads when excited by the building voltage compared to the sinusoidal condition.

Table 4.3. Impact of 5% THDv Building Voltage Compared to Sinusoidal Voltage.

Load	THDi	
	Increase	Decrease
Incandescent lamp	X	
Box fan	X	
Refrigerator	X	
T8 fluorescent, electronic ballast		X
T12 fluorescent, electronic ballast		X
T12 fluorescent, magnetic ballast	X	
Window AC, compressor & fan	X	
Microwave oven	X	
Window AC, fan only		X
Compact fluorescent lamp (five bulbs)		X
Personal computer, without monitor		X

All the ‘decrease’ cases are power electronic loads including the fan of the window air conditioner. Thus, one cannot automatically conclude that a distorted voltage increases THDi, except in the case of a resistive load or other nearly linear load.

4.1.5 Test Results Using One Voltage Harmonic

The sensitivity of load THDi to fundamental plus one voltage harmonic was investigated for all odd harmonics through the 25th multiple with cosine phase angle reference 0º (peaky), 90º (skewed left), 180º (flattened), and 270º (skewed right) for each of the eleven test loads. The tests were made using single harmonic voltage magnitudes of 10%, except for the microwave oven where 5% of the fundamental was used.

Each of the following ten graphs contain forty-nine individual measurements (four points for each of the twelve odd harmonics 3, 5, …, 25), plus a dashed line that indicates THDi for the sinusoidal voltage case. To simplify the interpretation of the findings, the upper and lower envelopes of the measured THDi are plotted with solid lines, the reference sinusoidal voltage THDi is represented by the dashed line, and comments are added where needed.

The incandescent lamp is a purely resistive load and is directly responsive to the 10% voltage distortion regardless of harmonic or phase angle. The results are not shown here because the load behaved exactly as expected, i.e., the harmonic voltage induces the same harmonic current, and the THDi is equal to the THDv of the exciting voltage.

4.1.5.1 Box Fan

As seen in Figure 4.6, the box fan is more responsive to low harmonic voltages which cause greater current distortion than the sinusoidal reference case (dashed line) for all phase angles. The box fan induces current harmonic k when subjected to voltage harmonic k. Compared to the sinusoidal voltage reference case, the flattened 3rd harmonic voltage causes four times greater THDi, while peaky 3rd harmonic voltage causes three times greater THDi. As the voltage harmonic order increases, the THDi exponentially decays back to the reference. The inductance of the fan acts as a filter choking the high-order harmonics.

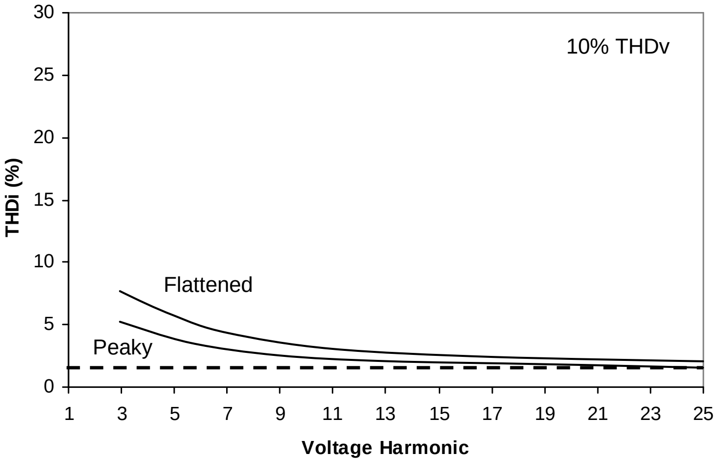


Figure 4.6. Box fan.

4.1.5.2 Refrigerator

Similar to the box fan, the refrigerator is most affected by low-order voltage harmonics which cause greater distortion than the reference case for all phase angles as seen in Figure 4.7. Harmonic exciting voltages induce mostly 3rd harmonic current. The peaky 3rd harmonic voltage causes the THDi to be five times greater than the reference case, while the flattened 3rd harmonic voltage causes the THDi to be three times greater than the reference. The induced THDi exponentially decreases back to the reference case as the voltage harmonic order increases.

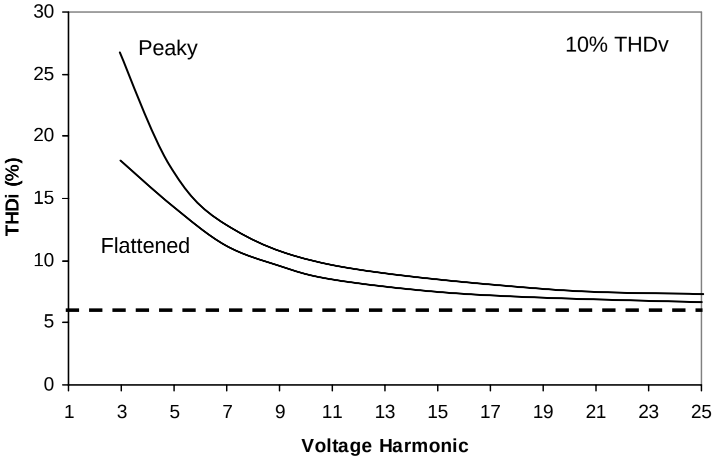


Figure 4.7. Refrigerator.

4.1.5.3 T8 Fluorescent Lamp with Electronic Ballast

The THDi of the T8 fluorescent lamp with electronic ballast is relatively independent of harmonic voltage. Voltage harmonics induce mostly 3rd harmonic currents which decrease in magnitude as the voltage harmonic order increases. When low-order voltage harmonics excite the load, the range of THDi expands depending on the phase angle of the voltage harmonic. The THDi of the peaky 3rd harmonic voltage is approximately two times greater than the reference case; however, the THDi of the flattened 3rd harmonic voltage is approximately half of the reference case seen in Figure 4.8. The opposite is true for the 5th harmonic. When the 5th harmonic is peaky, the THDi is at the lower bound of the envelope, while the flattened voltage causes the THDi to be at the upper bound. This pattern alternates for every odd harmonic, as the THDi exponentially converges to an asymptote slightly above the reference case THDi.

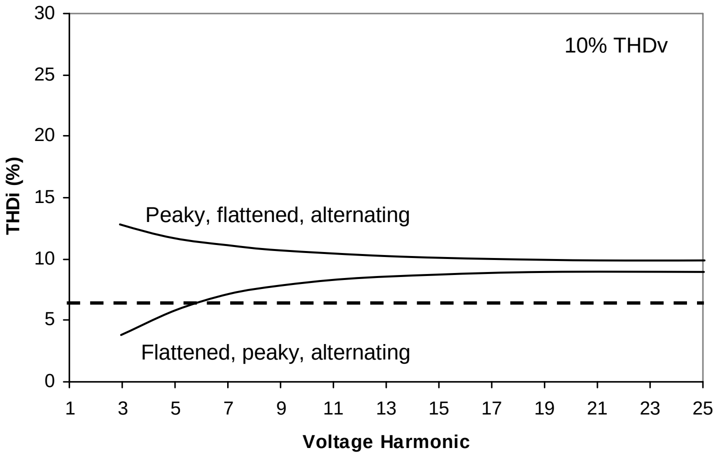


Figure 4.8. T8 fluorescent lamp with electronic ballast.

4.1.5.4 *T12 Fluorescent Lamp with Electronic Ballast*

In the T12 fluorescent lamp with electronic ballast, the harmonic exciting voltages induce mostly the 3rd and 5th harmonic currents which are greatly amplified when subjected to peaky 3rd or 5th harmonic voltages. The peaky 3rd harmonic voltage produces twice as much THDi as the reference, while the flattened 3rd harmonic decreases the THDi to half of the reference case as shown in Figure 4.9. As the voltage harmonic order increases, the THDi becomes independent of harmonic order and converges exponentially to the reference THDi.

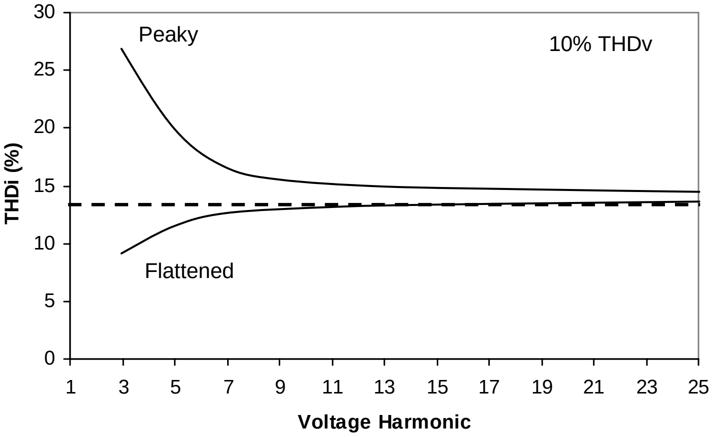


Figure 4.9. T12 fluorescent lamp with electronic ballast.

4.1.5.5 T12 Fluorescent Lamp with Magnetic Ballast

Harmonic excitation voltages induce mostly the 3rd and 5th current harmonics in the magnetic ballast of the T12 fluorescent lamp. The effect is more pronounced for 3rd and 5th voltage harmonics and sharply drops off above the 7th harmonic. The flattened 3rd harmonic voltage causes the THDi to be almost twice as large as the reference case, while the peaky 3rd harmonic voltage decreases the THDi by half of the reference case. The opposite is true for the 5th harmonic voltage; the peaky harmonic causes more THDi, while the flattened harmonic reduces the THDi compared to the reference case. The alternating pattern continues out to the 25th harmonic, as is common in magnetizing loads where the harmonic flux can cause the core to saturate. The THDi envelope shown in Figure 4.10 exponentially converges to the reference case as voltage harmonic order increases.

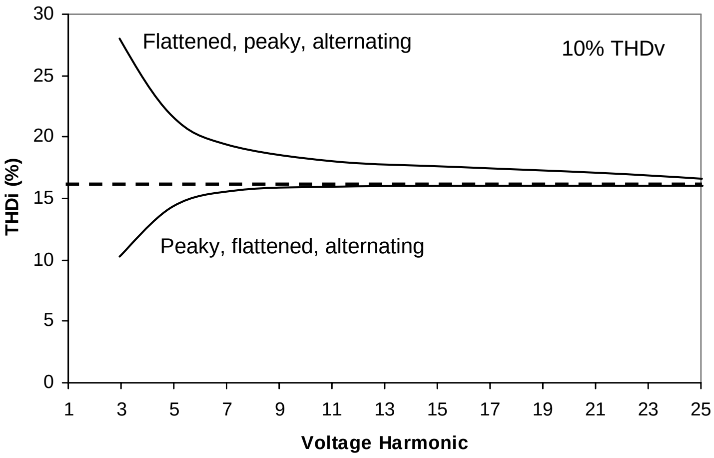


Figure 4.10. T12 fluorescent lamp with magnetic ballast.

4.1.5.6 Window Air Conditioner

Harmonic excitation voltage induces mostly the 3rd and 5th harmonic currents. However, as the voltage harmonic order increases, the 3rd and 5th harmonic currents decrease. This causes the THDi to exponentially decay to the reference case for high-order voltage harmonics as seen in Figure 4.11. The THDi is especially impacted by the low-order voltage harmonics. The 5th harmonic voltage causes a resonance in the compressor increasing the THDi by approximately a factor of two for all phase angles of harmonic voltage. In all cases, a peaky voltage causes the THDi to be at the upper bound of the envelope while a flattened voltage results in the lower bound.

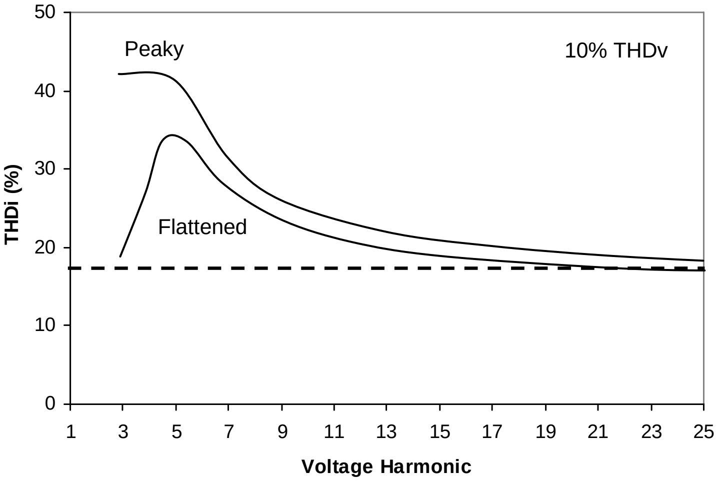


Figure 4.11. Window air conditioner.

4.1.5.7 Microwave Oven

In the case of the microwave oven, the exciting voltage harmonics induce all odd harmonic currents, which then decrease in magnitude as the voltage harmonic order increases. This causes the THDi to be relatively independent of voltage harmonic order. The 3rd harmonic voltage causes a slight variation in THDi from the reference case; skewed left harmonic voltage increases the THDi, and skewed right harmonic voltage decreases the THDi by approximately 20% as seen in Figure 4.12. The 5th and higher voltage harmonics have an insignificant effect on THDi compared to the reference case.

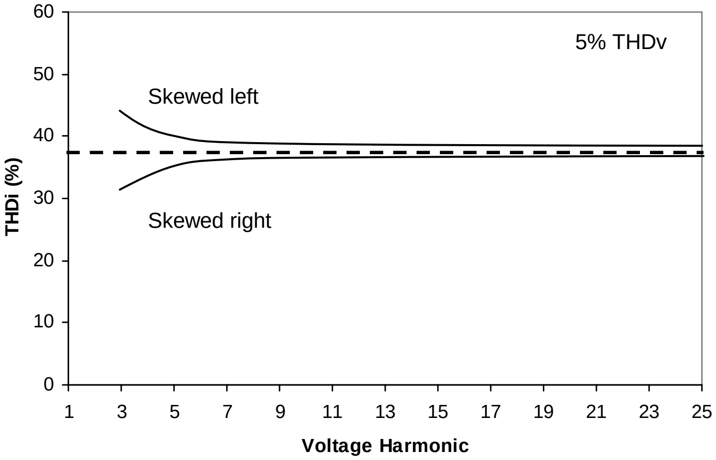


Figure 4.12. Microwave oven.

4.1.5.8 *Window Air Conditioner (Fan only)*

The fan of the window unit air conditioner is powered by a power electronic controlled DC motor. Harmonic exciting voltages induce primarily the 3rd and 5th harmonic currents. Shown in Figure 4.13, the peaky 3rd harmonic voltage increases the THDi by 20%, while the flattened 3rd harmonic voltage decreases the THDi by 20% from the reference case. The opposite is true for the 5th harmonic voltage – i.e., the flattened 5th harmonic voltage increases the THDi while the peaky 5th harmonic voltage decreases the THDi compared to the reference case. This alternates for every odd harmonic and exponentially converges to the reference THDi.

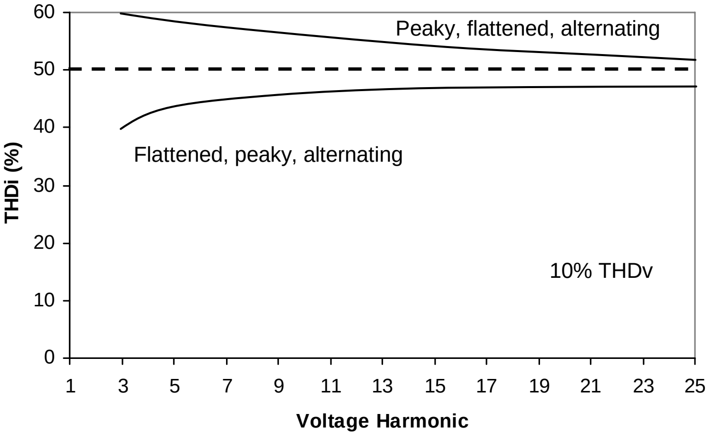


Figure 4.13. Window air conditioner (fan only).

4.1.5.9 Compact Fluorescent Lamp

Excitation voltage harmonic k induces the 3rd, 5th, Ik-2, Ik, and Ik+2 harmonic currents. The high-order exciting voltage harmonics have a more pronounced effect on THDi due to their impact on the Ik-2, Ik, and Ik+2 harmonic currents. In Figure 4.14, the load THDi is greater than the reference case for peaky 3rd harmonic voltage, and less than the reference case for flattened 3rd harmonic voltage. As the voltage harmonic order increases, the overall THDi increases; however, the phase of the exciting harmonic greatly affects the THDi within the envelope oscillating between the upper and lower bounds. For high excitation harmonics, the THDi is nearly twice as large as the reference case.

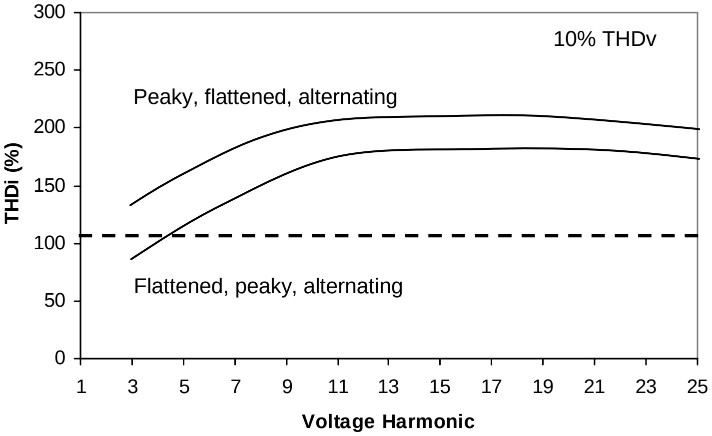


Figure 4.14. Compact fluorescent lamp.

4.1.5.10 Personal Computer

In the PC, low-order exciting voltage harmonics induce low-order harmonic currents, while the high-order exciting voltage harmonics induce a broad range of harmonic currents. When the load is excited by low-order harmonics, the resulting THDi is significantly different for different phase angles as seen in Figure 4.15. For the 3rd and 5th harmonic voltages, peaky harmonics increase the THDi, while flattened harmonics decrease the THDi from the reference case. Peaky harmonic voltages up to the 13th cause the load current to be one single narrow pulse each power frequency half cycle. After the 13th harmonic, the peaky voltage causes the current pulse to break into multiple conductions, therefore decreasing the THDi. Once that occurs, the phase angle of the voltage harmonic becomes less significant resulting in a convergence of the peaky and flattened THDi envelope. The THDi is greater than the reference case for high-order harmonic voltages.

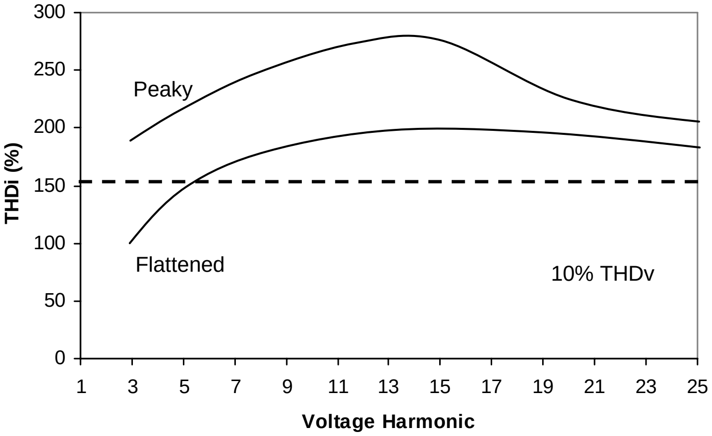
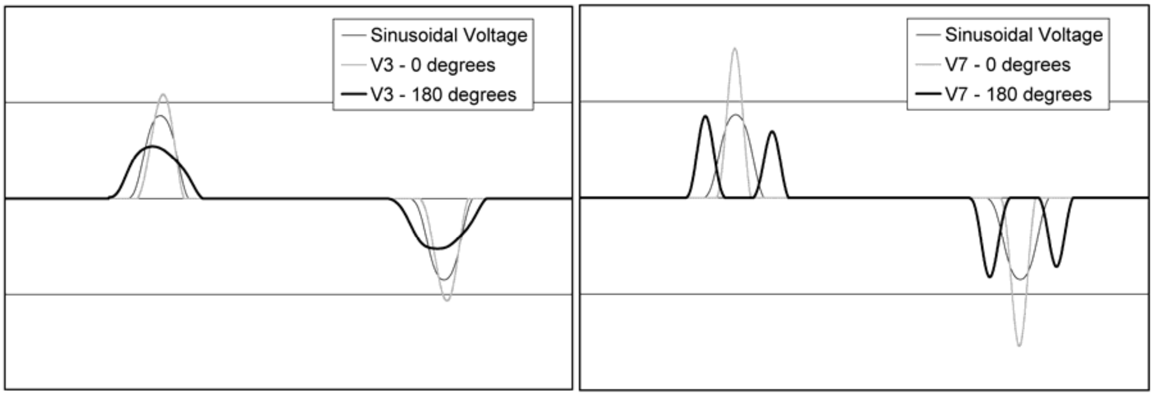


Figure 4.15. Personal computer.

The peaky 3rd harmonic voltage generates more THDi, while the flattened 3rd harmonic voltage allows the load to conduct for a longer period of time, generating less

THDi than the reference. This can be seen in Figure 4.16a for one power frequency cycle where the peaky voltage causes a narrow current pulse with increased amplitude while the flattened voltage causes a wider current pulse with decreased amplitude compared to the sinusoidal case.

In Figure 4.16b the load breaks into a double conduction mode for the flattened 7th harmonic. This allows the load to conduct for two intervals with decreased amplitude while the peaky 7th harmonic voltage causes the load to conduct for one short interval every half cycle. Therefore, more THDi is generated for the peaky case compared to the flattened case.



(a) (b)

Figure 4.16. One cycle of load current for the PC excited by nearly sinusoidal, peaky, and flattened (a) 3rd harmonic voltage and (b) 7th harmonic voltage (same scale in both graphs).

4.1.6 Summary

This chapter section gives the results of extensive harmonic testing on eleven common 120Vac, 60Hz, single-phase loads. The loads are tested with sinusoidal voltage excitation, a simulated building voltage waveform with 5% THDv, and fundamental plus individual odd harmonics 3rd, 5th, …, 25th multiples with either 10% or 5% THDv and controlled phase angles. To achieve the desired voltage excitation, an inverter-based testing station with precision load voltage feedback correction is employed.

THDi results obtained by using the 5% simulated building voltage are very similar to those obtained with sinusoidal excitation. Contrary to what might be expected, the THDi of electronic loads such as a personal computer actually decreases when the simulated building voltage is used because of the characteristic flattened waveshape of that voltage. This is also seen in the individual test for flattened 3rd harmonic voltage.

The variation of THDi with harmonic voltage magnitude and phase angle depends greatly on load type. For all except the high-distorting loads, the 3rd harmonic voltage has the greatest impact on THDi.

Load response depends largely on the phase angle of the harmonic voltage. This is especially true for the 3rd and 5th harmonic voltages, whose phase shift has a significant impact on the peaky or flattened nature of the composite voltage. The THDi of some loads is considerably worse with peaky voltage excitation – e.g., refrigerator, T12 electronic ballast, window air conditioner, and PC. Other loads have an alternating peaky/flattened pattern of THDi sensitivity – e.g., T8 electronic ballast, T12 magnetic ballast, window air conditioner (fan only), and compact fluorescent light.

Two loads experienced serious resonance – the refrigerator near the 3rd harmonic, and the window air conditioner near the 3rd and 5th harmonics. There is a significant increase in THDi near those harmonics. The power consumed by these loads increases by 7 and 3 percent, respectively. This increase manifests itself as additional motor losses.

4.2 PROBLEMS IN THE USE OF NORTON EQUIVALENT MODELS FOR SINGLE-PHASE NONLINEAR LOADS

4.2.1 Introduction

The use of Norton equivalent models for composite customer loads has been widely discussed [19-21]. However, as explained in most circuit analysis textbooks, Norton equivalents are intended to be used only with linear circuits and loads. For a Norton equivalent to be valid, its complex impedance and phasor current, $Z_{n,k}$ and $I_{n,k}$, for any harmonic k should be constant and independent of the applied voltage waveshape. Our measurements show that neither $Z_{n,k}$ or $I_{n,k}$ are constant enough to justify the use of Norton equivalents for nonlinear loads.

The Norton equivalent model is shown in Figure 4.17. Its parameters for a harmonic k can be experimentally determined using two sets of voltage and current measurements $V_k^{(1)}$, $I_k^{(1)}$ and $V_k^{(2)}$, $I_k^{(2)}$.

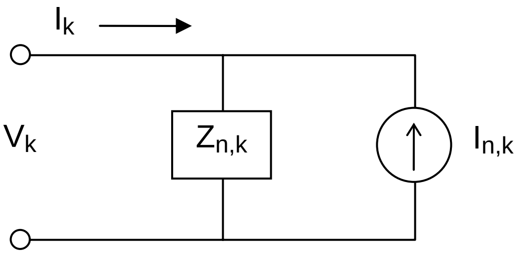


Figure 4.17. Norton equivalent load model.

The two sets of measurements, together with

$$Z_{n,k} = \frac{V_k^{(2)} - V_k^{(1)}}{I_k^{(2)} - I_k^{(1)}} \tag{4-10}$$

and

$$I_{n,k} = \frac{V_k^{(1)}}{Z_{n,k}} - I_k^{(1)} \tag{4-11}$$

are used to solve for $Z_{n,k}$ and $I_{n,k}$. The fundamental voltage phase angle must be the same in both experiments. In our tests we obtained the sets of V_k, I_k using the Harmonics Testing Station illustrated in Figure 4.1.

4.2.2 Test Loads

The four test loads from Table 4.1 used to evaluate the Norton equivalent load models are listed in Table 4.4. The personal computer and compact fluorescent lamp are highly nonlinear loads. They have severe current distortion whose harmonics change significantly with voltage waveshape. The window air conditioner is representative of a significant portion of summer peak load and has a slight nonlinearity that causes noticeable interaction between voltage and current harmonics. The incandescent lamp, which obviously is a linear load, is used as a benchmark to confirm our testing and calculation procedures.

Table 4.4. Norton Equivalent Test Loads.

Load	THDi (%) *	Power (W)
Personal computer, without monitor	152	34
Compact fluorescent lamp (four bulbs)	107	52
Window air conditioner	17	488
Incandescent lamp	1	213

* THDi for sinusoidal voltage excitation.

4.2.3 Waveforms and Waveform Interaction

4.2.3.1 Load Voltage

The waveforms we used are:

1. Sinusoidal voltage.
2. Simulated building voltage having THDv = 5% and a typical building voltage waveshape (Figure 4.3) and harmonic content (Table 4.2).
3. Sinusoidal voltage plus 5% of 3rd, 5th, or 7th harmonic voltage with phase angle either peaky (P) or flattened (F).

4.2.3.2 Load Current

The voltage waveform has a significant impact on the harmonic content of nonlinear load currents. In a linear load, such as the incandescent lamp, the introduction of harmonic voltage induces a proportional change in harmonic current. For a nonlinear load, however, the complete current harmonic spectra and respective phase angles change out-of-proportion and out-of-phase with the applied harmonic voltages.

Consider Figure 4.18. The load current of the personal computer changes with voltage waveshape. A sinusoidal voltage produces a taller and narrower current pulse than does the flattened building voltage waveform.

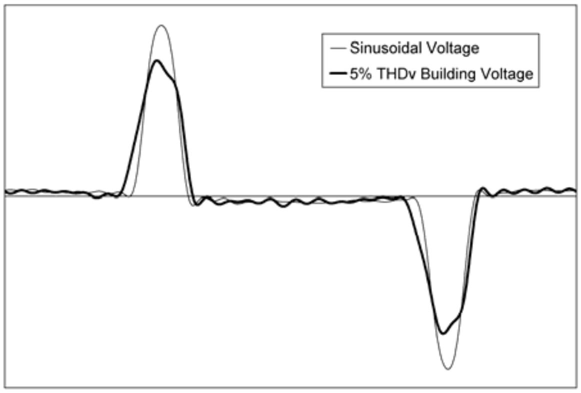


Figure 4.18. One cycle of personal computer current excited by sinusoidal and 5% THDv simulated building voltage.

The current of the compact fluorescent lamp shown in Figure 4.19 on the following page is also impacted by voltage distortion. The flattened nature of the building voltage causes the load to conduct for a longer period with increased harmonics than does the sinusoidal voltage waveform.

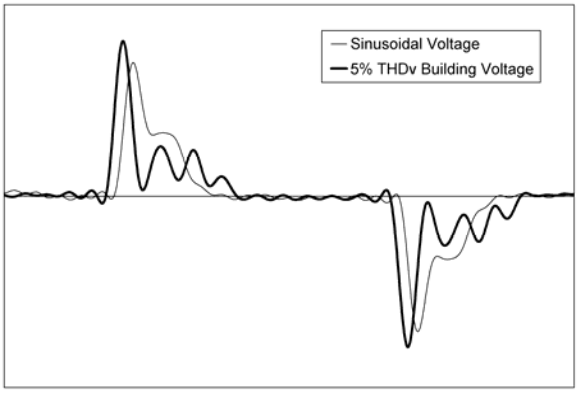


Figure 4.19. One cycle of compact fluorescent lamp current excited by sinusoidal and 5% THDv simulated building voltage.

The window air conditioner has a slight non-linearity due to magnetic saturation and a small DC fan motor drive. As shown in Figure 4.20, the load current changes significantly with voltage.

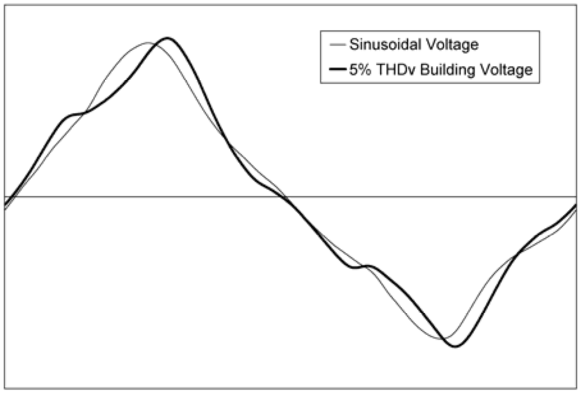


Figure 4.20. One cycle of window air conditioner current excited by sinusoidal and 5% THDv simulated building voltage.

Figures 4.18, 4.19, and 4.20 each represent a pair of experiments that can be used with (4-10) and (4-11) to compute Norton equivalents. These three Norton equivalents will exactly reproduce the results in Figures 4.18, 4.19, and 4.20. Unfortunately, as we will show in the next section, the Norton model parameters are a function of voltage waveshape and, in general, are accurate only for the two experiments used to compute them.

4.2.4 Test Results

We performed two different types of harmonic tests. In single harmonic tests, we excited the load with 120Vrms, 60Hz plus 5% of 3rd, 5th, or 7th peaky or flattened voltage. In the mixed harmonic tests, we used the 5% THDv building voltage waveform shown in Figure 4.3.

At this point, it is helpful to explain the purpose of testing the incandescent lamp. The incandescent lamp has a known resistance and zero Norton current. Knowing this, we were able to ascertain that accuracy in Norton model calculations requires harmonic voltage changes in (4-10) of approximately 1% or greater. Therefore, we have limited our analysis and conclusions to tests where the complex difference between $V_k^{(1)}$ and $V_k^{(2)}$ is 1% or greater.

In this section, we discuss the key findings and point out the deficiencies of using the Norton model for nonlinear loads. The complete set of Norton results are shown in Appendix A, and the complete set of voltage and current spectra are shown in Appendix B.

4.2.4.1 Personal Computer

The 3rd harmonic Norton parameters for the personal computer are given in Table V. The eight voltage test waveforms are paired into ten sets of $V_k^{(1)}$, $I_k^{(1)}$ and $V_k^{(2)}$, $I_k^{(2)}$ for use in (4-10) and (4-11). In the 'Waveform 1' and 'Waveform 2' columns, the notation 'P' means peaky single harmonic voltage, 'F' means flattened single harmonic voltage, and 'BV' means simulated building voltage. 'Sgl' indicates the results are determined with single harmonic waveforms, while 'Mixed' indicates the results are determined when one waveform is the simulated building voltage.

Table 4.5. Personal Computer 3rd Harmonic Norton Load Model (sine angles).

Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang
Sinusoidal	5% V3, P	Sgl	431	-151	0.393	-1
Sinusoidal	5% V3, F		5700	69	0.393	-1
5% V3, P	5% V3, F		897	-153	0.384	0
5% BV	Sinusoidal	Mixed	30	-55	0.396	-1
5% BV	5% V3, P		66	-69	0.349	-20
5% BV	5% V3, F		11	60	1.040	-41
5% BV	5% V5, P		31	-57	0.387	0
5% BV	5% V5, F		27	-69	0.344	7
5% BV	5% V7, P		32	-54	0.396	-2
5% BV	5% V7, F		29	-84	0.275	4

For any given row in Table 4.5, the values Z3_mag, Z3_ang, I3_mag, and I3_ang satisfy (4-10) and (4-11) exactly for the circuit in Figure 4.17 using the two voltage waveforms indicated as ‘Waveform 1’ and ‘Waveform 2.’ If Norton modeling is valid for the personal computer, then every row of Norton impedance and current in the above table would be nearly identical. However, there is considerable variation, especially in the impedance of the top six rows.

Based upon the results in Table 4.5, our conclusions for the personal computer are as follows:

- Norton models for ‘Mixed’ harmonic tests vary too much to be useful.
- ‘Sgl’ harmonic tests produce mostly steady Norton currents, but the Norton impedance magnitudes and angles vary greatly.
- Two tests yield negative Norton resistances (i.e., Z3_ang of -151 and -153 degrees).

The Norton inaccuracies described above are not unique to the 3rd harmonic. The same inaccuracies are also evident in the results for the 5th and 7th harmonics as shown in Tables 4.6 and 4.7, respectively.

Table 4.6. Personal Computer 5th Harmonic Norton Load Model (sine angles).

Waveform 1	Waveform 2		Z5_mag	Z5_ang	I5_mag	I5_ang
Sinusoidal	5% V5, P	Sgl	403	-37	0.342	178
Sinusoidal	5% V5, F		64	23	0.342	178
5% V5, P	5% V5, F		118	16	0.291	-176
5% BV	Sinusoidal	Mixed	13	-31	0.335	178
5% BV	5% V3, P		12	-31	0.350	-179
5% BV	5% V3, F		13	-35	0.318	-179
5% BV	5% V5, P		37	-45	0.255	140
5% BV	5% V5, F		16	84	0.561	120
5% BV	5% V7, P		12	-26	0.369	177
5% BV	5% V7, F		13	-82	0.082	-153

Table 4.7. Personal Computer 7th Harmonic Norton Load Model (sine angles).

Waveform 1	Waveform 2		Z7_mag	Z7_ang	I7_mag	I7_ang
Sinusoidal	5% V7, P	Sgl	129	-8	0.276	-4
Sinusoidal	5% V7, F		21	8	0.278	-4
5% V7, P	5% V7, F		36	6	0.111	8
5% BV	Sinusoidal	Mixed	5	0	0.283	-3
5% BV	5% V3, P		5	-4	0.285	3
5% BV	5% V3, F		5	-25	0.191	22
5% BV	5% V5, P		5	7	0.334	-5
5% BV	5% V5, F		6	-37	0.103	23
5% BV	5% V7, P		26	-26	0.159	-71
5% BV	5% V7, F		25	52	0.242	-69

4.2.4.2 Compact Fluorescent Lamp

The 3rd harmonic Norton load models for the compact fluorescent lamp are given in Table 4.8.

Table 4.8. Compact Fluorescent Lamp 3rd Harmonic Norton Load Model (sine angles).

Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang
Sinusoidal	5% V3, P	Sgl	59	2	0.614	83
Sinusoidal	5% V3, F		57	-25	0.613	83
5% V3, P	5% V3, F		59	-12	0.580	82
5% BV	Sinusoidal	Mixed	33	-68	0.612	83
5% BV	5% V3, P		57	-44	0.514	78
5% BV	5% V3, F		15	8	0.674	42
5% BV	5% V5, P		24	-24	0.642	65
5% BV	5% V5, F		59	-113	0.493	93
5% BV	5% V7, P		24	-11	0.607	60
5% BV	5% V7, F		54	-78	0.529	86

Overall, for the compact fluorescent lamp, we conclude that

- Norton models for ‘Mixed’ harmonic tests vary too much to be useful.
- ‘Sgl’ harmonic tests produce steady Norton models.
- One test (i.e., fifth row of ‘Mixed’ results) has a negative resistance.

Results for the 5th and 7th harmonic tests yield the same conclusions.

4.2.4.3 *Window Air Conditioner*

The window air conditioner is more linear than the computer and compact fluorescent lamp; however, the Norton model is not consistent. The 3rd harmonic Norton models are shown in Table 4.9.

Table 4.9. Window Air Conditioner 3rd Harmonic Norton Load Model (sine angles).

Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang
Sinusoidal	5% V3, P	Sgl	15	24	0.940	-72
Sinusoidal	5% V3, F		11	12	0.943	-72
5% V3, P	5% V3, F		13	17	0.946	-79
5% BV	Sinusoidal	Mixed	10	21	0.940	-72
5% BV	5% V3, P		12	21	0.895	-80
5% BV	5% V3, F		21	29	0.919	-98
5% BV	5% V5, P		9	36	1.160	-73
5% BV	5% V5, F		19	16	0.834	-95
5% BV	5% V7, P		13	40	1.070	-87
5% BV	5% V7, F		10	33	1.070	-77

Overall, for the window air conditioner, our conclusions are that

- Norton models for ‘Mixed’ harmonic tests vary too much to be useful.
- ‘Sgl’ harmonic tests indicate steady Norton models.

The conclusions for the 5th and 7th harmonic tests are the same.

4.2.4.4 *Incandescent Lamp*

The incandescent lamp results in Appendix A confirm the instrumentation and testing procedure. The Norton impedance is correct and the Norton current is zero. However, because of subtraction errors in (4-10), the results become less accurate when the harmonic voltage change in (4-10) is 1% (see boxed ‘Mixed’ 7th harmonic results where the change in 7th harmonic voltage is approximately 1%).

4.2.5 Summary

Norton models for the personal computer, compact fluorescent lamp, and window air conditioner depend greatly on voltage waveshape. There is a wide range of Norton parameters for any one of these loads depending on the voltage waveforms used in the calculations. In some cases, the Norton impedance even has a negative resistance.

Norton equivalents are intended to be used with linear circuits. Our tests show they are inappropriate for even mildly-nonlinear loads such as a window air conditioner.

If Norton equivalents are inappropriate for building block single-phase nonlinear loads, they are most likely inappropriate for composite nonlinear loads and three-phase nonlinear loads. If so, one should then ask the following two questions:

1. Which two sets of voltage and current measurements are to be used in computing the Norton model?
2. In practice, how does one create a significant (≥ 1%) change in harmonic voltage so that the measurements can be made?

In our opinion, the above two questions must be addressed before a serious attempt is made to use Norton equivalent models to determine a customer's impact on the power system.

Chapter 5 – Power Electronic Transient Load Model

Single-phase power electronic loads require power from the AC system for a short interval near the peak of the voltage waveform. During the rest of the cycle, the power electronic load is effectively disconnected from the system; however, the connected DC load still requires constant power. This constant power is delivered from the DC load capacitor.

Power electronic loads are typically constant power in steady state; however, transients occur at the onset and clearing of voltage sags. At the onset of a significant voltage sag, the power electronic load effectively disconnects from the system and its DC capacitor provides ride-through power. During the voltage sag, the DC capacitor voltage decays to a new steady state as energy is discharged into the load. As the voltage decays, load can slowly reconnect to the system. After the voltage sag ends, the load then requires additional power to recharge the DC capacitor.

Using switching models or actual dynamics of power electronic loads in large-signal transient simulations will require vast computer resources and extensive simulation times; therefore, averaging techniques are used to model the power electronic load. Although the AC current waveform is rich in harmonics, only the fundamental is participating to produce real power. Thus, the composite load is modeled at the network bus as the fundamental average power. This chapter develops the transient load model for the average system power drawn by the composite power electronic load.

5.1 INDIVIDUAL POWER ELECTRONIC LOAD

The dynamics of individual single-phase power electronic loads can be described using a simple capacitor-filtered diode-bridge rectifier (DBR) model. A circuit diagram of this model can be seen in Figure 5.1.

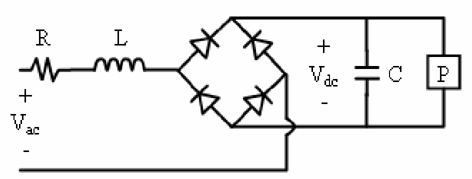


Figure 5.1. Circuit diagram for single-phase power electronic load.

The power electronic load capacitor *C* experiences a restoring and discharging interval every half cycle. As shown in Figure 5.2 for half a 60Hz power frequency cycle, the capacitor voltage is initially above the source voltage. This reverse biases the diode bridge and therefore causes the capacitor to discharge into the load. At the moment the absolute value of source voltage is greater than the capacitor voltage, the diodes are forward biased and capacitor begins to restore. In Figure 5.2, the restoration is delayed due to system inductance. After the source voltage drops below the capacitor voltage and the current in the line goes to zero, the capacitor begins to discharge again.

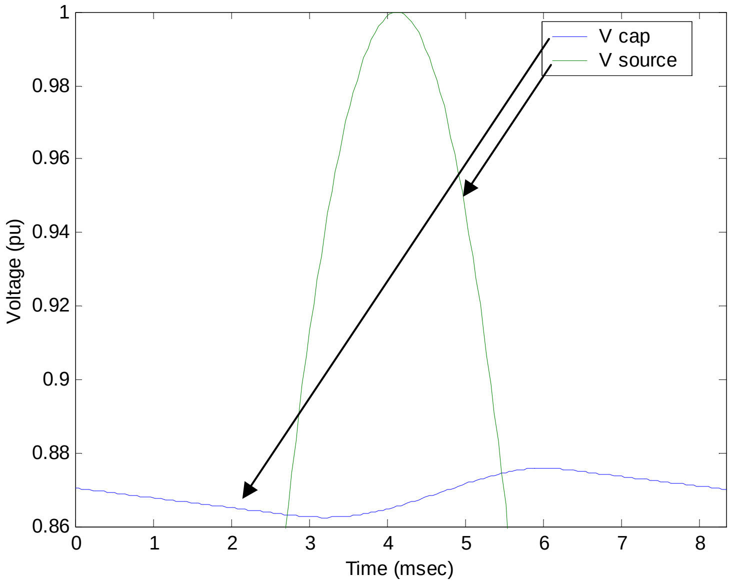


Figure 5.2. Power electronic load DC capacitor voltage steady state response to AC source voltage.

When the initial voltage $V_{cap}(t = 0\text{msec})$ and final voltage $V_{cap}(t = 8.33\text{msec})$ in Figure 5.2 are equal, the load is in steady state. The steady state voltage of the power electronic load can be found by using the circuit dynamic equations and varying the initial voltage. The differential equations describing the restoring and discharging intervals are given in (5-1) and (5-2), respectively.

$$V_{ac}(t) = LC\frac{d^2V_{dc}(t)}{dt^2} + \left(RC - \frac{LP}{V_{dc}^2(t)}\right)\frac{dV_{dc}(t)}{dt} + \frac{RP}{V_{dc}(t)} + V_{dc}(t) \tag{5-1}$$

$$V_{dc}(t)\cdot C\frac{dV_{dc}(t)}{dt} = -P \tag{5-2}$$

Typically, $RC >> \frac{LP}{V_{dc}^2(t)}$ and $\frac{RP}{V_{dc}(t)} << V_{dc}(t)$, by at least two orders of magnitude, so (5-1) reduces to

$$V_{ac}(t) = LC\frac{d^2V_{dc}(t)}{dt^2} + RC\frac{dV_{dc}(t)}{dt} + V_{dc}(t). \tag{5-3}$$

Solving these differential equations using the Laplace transform [22], one can determine the continuous time domain solution for the capacitor voltage.

The time domain solution for the restoring interval (5-3) is

$$\begin{aligned} V_{dc}(t) = {} & \frac{V_p \cos(\theta)}{LC}[\mathbf{B}] + \frac{V_p \sin(\theta)}{LC}[\mathbf{A}] + \left[\frac{RV_{dc}(0)}{L} - \frac{I_{cap}(0)}{C}\right]\left[\frac{1}{(\omega_1 - \omega_2)}\right]\left[e^{-\omega_2 t} - e^{-\omega_1 t}\right] \\ & + V_{dc}(0)\left[\frac{1}{(\omega_1 - \omega_2)}\right]\left[\omega_1 e^{-\omega_1 t} - \omega_2 e^{-\omega_2 t}\right] \end{aligned} \quad . \qquad (5\text{-}4)$$

when $\omega_1 \neq \omega_2$, and

$$V_{dc}(t) = \frac{V_p \cos(\theta)}{LC}[\mathbf{B}] + \frac{V_p \sin(\theta)}{LC}[\mathbf{A}] + \left[\frac{RV_{dc}(0)}{L} - \frac{I_{cap}(0)}{C}\right] \cdot te^{-\omega_1 t} + V_{dc}(0)[1 - \omega_1 t]e^{-\omega_1 t} \qquad (5\text{-}5)$$

when $\omega_1 = \omega_2$. V_p is the peak AC voltage; θ is the relative angle of the voltage sine wave when the restoring interval begins; variables [**A**] and [**B**] are defined in Appendix C; and

$$\omega_{1,2} = \frac{R/L \pm \sqrt{\left(\left(R/L\right)^2 - 4/LC\right)}}{2}. \qquad (5\text{-}6)$$

The associated system current during the restoring interval is $I_{ac}(t) = \frac{P}{V_{dc}(t)} + C\frac{dV_{dc}(t)}{dt}$.

The time domain solution for the discharging interval (5-2) is

$$V_{dc}(t) = \left(V_{dc}^2(0) - \frac{2Pt}{C}\right)^{1/2}, \qquad (5\text{-}7)$$

where load power *P* and DBR capacitance *C* dictate the DC capacitor storage factor. The storage factor β is defined as

$$\beta = \frac{C}{2 \cdot P}. \qquad (5\text{-}8)$$

Typical power electronic loads have approximately 5% DC voltage ripple. The approximate capacitor storage factor rating is calculated with (5-7) rearranged as

$$\beta = \frac{t}{V_{\max}^2 - V_{\min}^2} \qquad (5\text{-}9)$$

where *t* is the length of the discharging interval and V_{max} is the peak DC voltage. On a 120V system, the storage factor is approximately 3uF/W when V_{max} is the peak AC system voltage and *t* is half a power frequency cycle.

5.1.1 Individual Power Electronic Load Response During a Fault

The power electronic load can respond in several different ways during a fault depending on the pre-fault steady state capacitor voltage and the peak fault voltage. The transient response shown in Figure 5.3 occurs when the pre-fault steady state capacitor voltage is greater than the peak fault voltage. The load effectively disconnects from the system until the DC capacitor discharges to the peak fault voltage. During this time, the load remains energized by the DC capacitor. The length of time μ that the load rides-through the fault before reconnecting to the system is

$$\mu = \left(V_{capSSpf}^{2} - V_{peakf}^{2}\right) \cdot \beta \, . \tag{5-10}$$

The ride-through time μ is governed by the pre-fault steady state capacitor voltage $V_{capSSpf}$, system peak fault voltage V_{peakf}, and the load storage factor. In this case $\mu > 0$ and the DC capacitor provides ride-through power.

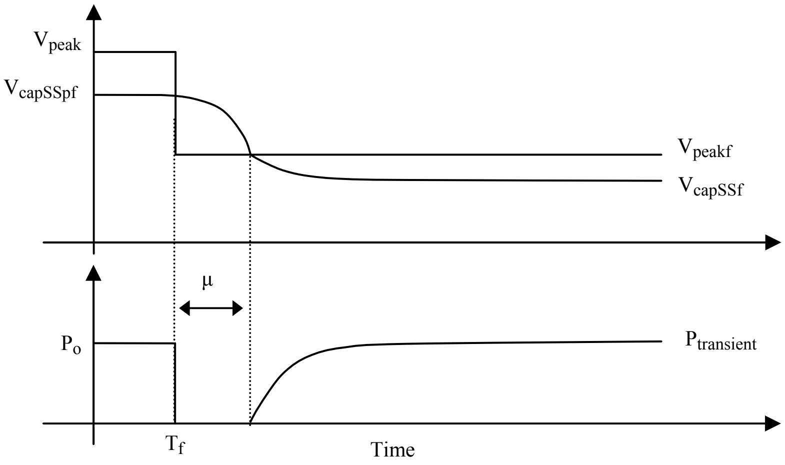


Figure 5.3. Peak system and DC capacitor voltage along with system power when power electronic load rides-through a portion of the fault (i.e., $\mu > 0$).

There is also the case that the peak fault voltage is greater than or equal to the steady state pre-fault capacitor voltage. Therefore by (5-10), $\mu \leq 0$. The load does not disconnect from the system, and the DC capacitor does not need to provide ride-through power. Instead, a portion of the load remains connected to the system. This transient response is shown in Figure 5.4.

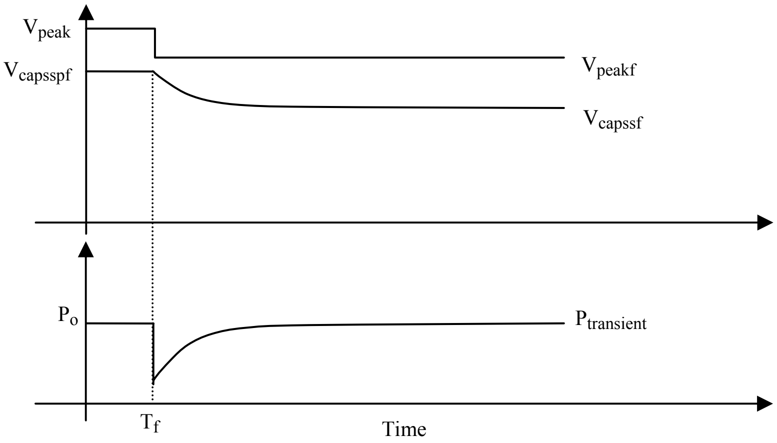


Figure 5.4. Peak system and DC capacitor voltage along with system power when power electronic load remains connected to the system in the fault (i.e., $\mu \leq 0$).

5.1.1.1 DC Capacitor Provides No Ride-Through ($\mu \leq 0$)

The power electronic load remains connected to the system during the complete fault when $\mu \leq 0$. This occurs when the peak fault voltage is greater than or equal to the pre-fault steady state capacitor voltage. The recovery of load can be determined by knowing the time constant τ_f of the power electronic capacitor voltage decay. The capacitor voltage decays to a new steady state as

$$V_{cap}(t) = V_{capSSf} + \left(V_{capSSpf} - V_{capSSf}\right) \cdot \exp\left(- t/\tau_f\right) \tag{5-11}$$

where V_{capSSf} is the steady state load capacitor voltage during the fault which is determined similarly to the pre-fault steady state capacitor voltage. The analytical dynamic equations (5-4), (5-5), and (5-7) are used to solve the capacitor voltage after a half power frequency cycle which includes the restoring and discharging interval. The fault time constant is solved by

$$\tau_f = -T/2 \Big/ \ln\left(\frac{V_{cap}(T/2) - V_{capSSf}}{V_{capSSpf} - V_{capSSf}} \right) \qquad (5\text{-}12)$$

where T is the period of the power frequency cycle. Figure 5.5 illustrates the exponential voltage decay compared to the actual dynamic capacitor voltage and the system absolute voltage. Time constant τ_f is approximately 0.04sec.

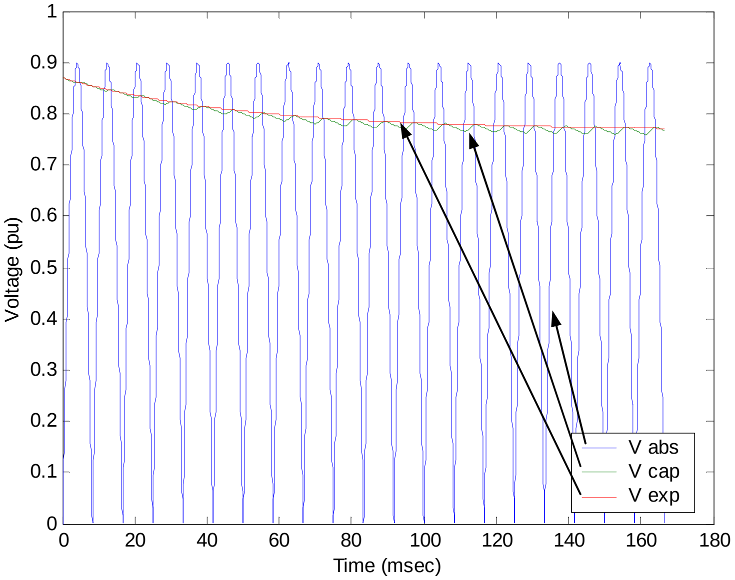


Figure 5.5. Exponential load capacitor voltage decay determined from differential equations during a fault.

As the load capacitor voltage decays to the new steady state, the load comes back online restoring for longer intervals, and the increasing voltage difference between the system and capacitor causes the system power to increase as seen in the bottom half of Figure 5.4. Referred to a DC system, the power would increase as

$$P(t) = V_{peakf} \cdot \frac{\left(V_{peakf} - V_{cap}(t)\right)}{R} \qquad (5\text{-}13)$$

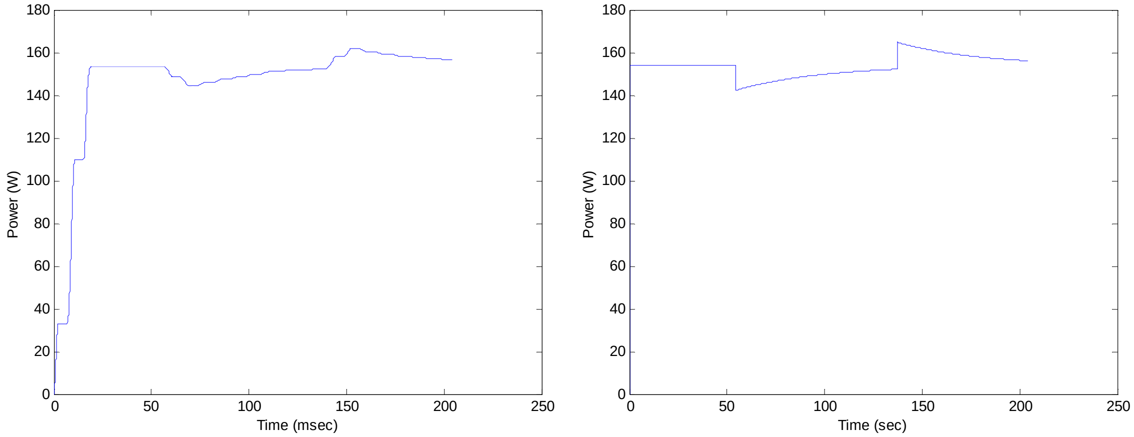
where V_{peakf} is the effective DC system fault voltage and R is the line resistance. The power electronic load transient response for system power therefore has the same time constant as voltage.

If the steady state pre-fault capacitor voltage is less than the peak fault voltage, a portion of the load will be served by the system at the onset of the fault. The power at the onset of the fault is approximately

$$P_{onset} \approx P_0 \cdot \frac{V_{peakf} - V_{capSSpf}}{V_{peakf} - V_{capSSf}} \tag{5-14}$$

where P_0 is the pre-fault steady state power. For example, a 1% voltage sag will hardly change the steady state capacitor voltage. The time constant to reach the new steady state, however, can be several cycles. The actual load online at the onset is near 100%. As the magnitude of sag increases, the amount of load connected at the onset would approach zero as μ approaches zero (i.e., $V_{capSSpf} = V_{peakf}$).

Using the actual dynamic equations (5-4), (5-5), and (5-7), and time averaging the actual system power using a one cycle moving window, the average power transient response for a 5% voltage sag can be seen in Figure 5.6a. Due to a low pass filtering effect caused by averaging the waveform, the initial power appears to increase and sudden transitions appear more gradual. At the onset of the fault, the majority of the load is supplied by to the system. For comparison, the onset power and fault time constant is determined using (5-12) and (5-14), and the power electronic model fault transient response is shown in Figure 5.6b. These responses are similar.



(a) (b)

Figure 5.6. Comparison of (a) average power provided by the system and (b) power electronic load model response using onset power.

5.1.1.2 DC Capacitor Provides Ride Through (μ > 0)

The steady state pre-fault capacitor voltage is greater than the peak fault voltage when μ > 0. The load effectively disconnects from the system for time μ while the DC capacitor supplies ride-through power to the load. When the capacitor voltage reaches the peak fault voltage, the load begins to draw system power. The increase in system power is directly proportional to the change in DC load capacitor voltage from the peak fault voltage to the steady state capacitor voltage in the fault. The capacitor voltage decays as

$$V_{cap}(t) = V_{capSSf} + \left(V_{peakf} - V_{capSSf}\right) \cdot \exp\left(- {t}/{\tau_f}\right). \qquad (5\text{-}15)$$

The exponential time constant τ_f can again be determined using (5-4), (5-5), and (5-7) solving the capacitor voltage after a half power frequency cycle as

$$\tau_f = -T/2 \Big/ \ln\left(\frac{V_{cap}(T/2) - V_{capSSf}}{V_{peakf} - V_{capSSf}}\right). \qquad (5\text{-}16)$$

As shown in Figure 5.3, when the capacitor voltage is above the peak fault voltage, the load power provided by the system is zero. The load recovers exponentially with time constant τ_f after the capacitor reaches the fault voltage.

5.2 COMPOSITE POWER ELECTRONIC LOAD

Power systems require that large numbers of individual loads be represented as a composite load at the network bus. The composite load transient response is also generated with (5-4), (5-5), and (5-7). For the composite load, the parameters in Figure 5.1 change because the individual loads are effectively in parallel. The capacitance and power increase while the system impedance (including source and load impedance) decreases. The composite load distribution is the average of the individual load responses and is represented as a Weibull cumulative density function (CDF) in the fault and an Exponential probability density function (PDF) after the fault clears. The Weibull CDF is chosen because the shape of the distribution can change depending on the ride-through time. The Weibull CDF can mimic an Exponential, Rayleigh, or Normal distribution.

5.2.1 Composite Power Electronic Load Response During a Fault

Power electronic loads with different storage factors can each have a different ride-through as indicated by μ_1, μ_2, and μ_3 in Figure 5.7. The composite load, indicated by the dashed line, has the average ride-through μ_4. The storage factor for the composite load is determined by the total power and capacitance of the three loads.

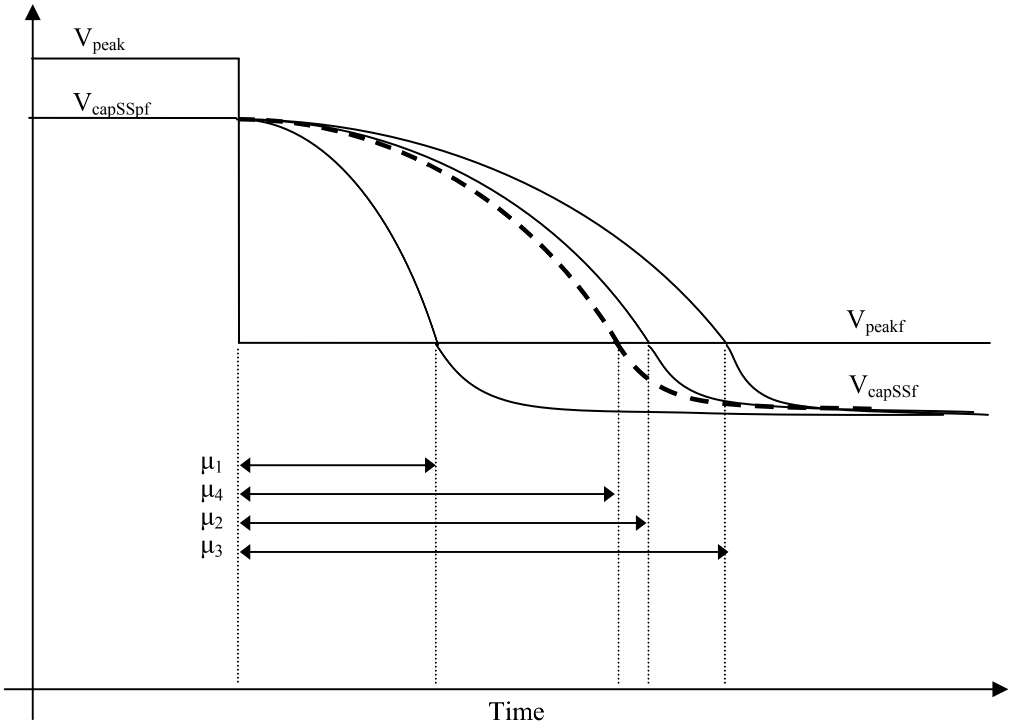


Figure 5.7. Individual load (solid lines) and composite load (dashed line) DC capacitor ride-through during a fault (i.e., $\mu > 0$).

An illustration of the composite load recovery and composite load Weibull CDF can be seen in Figure 5.8 when $\mu > 0$. The composite load distribution begins at the onset of the fault. Half the load reconnects to the system before time μ_4. However, although half the load is reconnected, it does not mean half the load is supplied by the system. Half the load is supplied by the system when the composite load (dashed line in Figure 5.7) reaches 50% of its path toward steady state after dropping below the peak fault voltage (i.e., 50% of the distributed load is provided by the system at $t = \mu_4 + \tau_f \cdot \ln(2)$). 99% of the composite load is provided by the system at approximately $5\tau_f$ after the composite load reconnects to the system (i.e., 99% of the distributed load is provided by the system at $t = \mu_4 + 5\tau_f$).

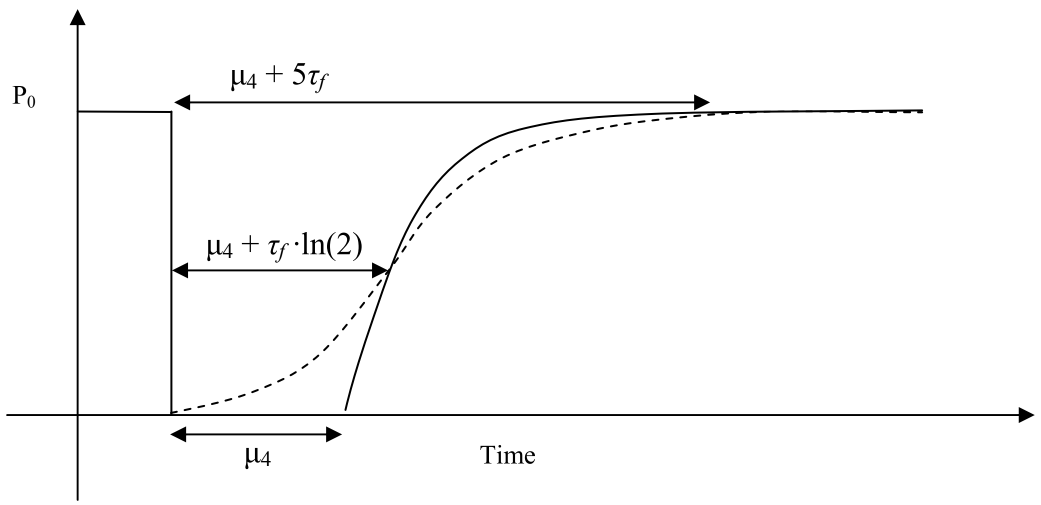


Figure 5.8. Composite load recovery (solid line) and composite load Weibull CDF (dashed line) during a fault.

The shape k and time constant λ of the Weibull CDF are determined by μ and τ_f. When $\mu \leq 0$, the shape of the Weibull CDF is exponential ($k = 1$) and $\lambda = \tau_f$. As μ increases greater than zero, the shape begins to mimic a Rayleigh or Normal CDF. The parameters of the Weibull CDF are calculated with the following two equations for the median and full load when $\mu > 0$.

$$0.5 = 1 - \exp\left(-\left(\frac{\tau_f \cdot \ln(2) + \mu}{\lambda}\right)^k\right) \tag{5-17}$$

$$0.99 = 1 - \exp\left(-\left(\frac{5 \cdot \tau_f + \mu}{\lambda}\right)^k\right) \tag{5-18}$$

Solving the system of equations, the Weibull λ and k are

$$\lambda = \exp\left(\frac{a/b \cdot \ln(5 \cdot \tau + \mu) - \ln\left(\tau_f \cdot \ln(2) + \mu\right)}{a/b - 1}\right) \tag{5-19}$$

$$k = a \Big/ \ln\left(\tau_f \cdot \ln(2) + \mu \Big/ \lambda\right) \tag{5-20}$$

where $a = \ln(\ln(2))$ and $b = \ln(\ln(100))$.

The composite power electronic load voltage sag response is a function of time starting at the onset of the fault T_f and lasting until fault clearing. Assuming the load does not shut-down due to low system voltage, the power electronic transient model is described as

$$P_f(t) = P_{onset} + (P_0 - P_{onset}) \cdot \left(1 - \exp\left(-\left(\frac{t - T_f}{\lambda}\right)^k\right)\right) \quad (5\text{-}21)$$

where $P_{onset} \approx P_0 \cdot \frac{V_{peakf} - V_{capSSpf}}{V_{peakf} - V_{capSSf}}$ when $\mu \le 0$ and $P_{onset} = 0$ when $\mu > 0$. If the load does shut-down due to low system voltage, $P_f(t) = 0$.

5.2.2 Composite Power Electronic Load After a Fault is Cleared

At the moment the fault is cleared, 100% of the power electronic loads are on-line consuming full load power. Because the load capacitors are no longer at the pre-fault steady state voltage, the loads require additional energy to recharge their capacitors back to steady state. Similar to the exponential voltage decay of the load capacitors during the fault, the voltage exponentially rises back to the pre-fault steady state. This response can be seen in Figure 5.9.

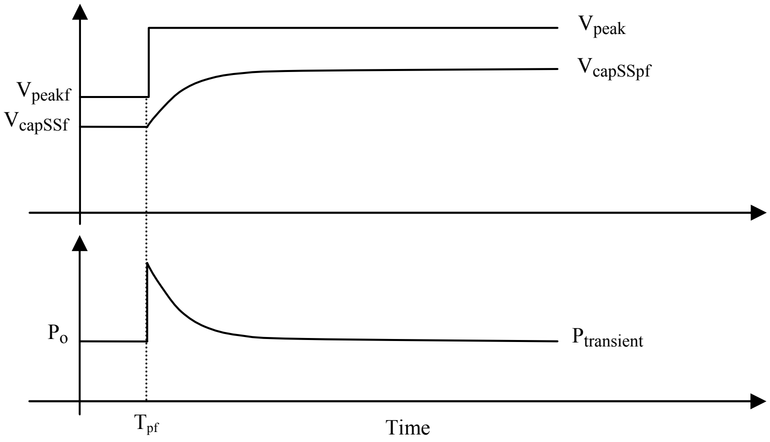


Figure 5.9. Peak system and DC capacitor voltage along with system power after the fault is cleared.

Using the capacitor voltage at the end of the fault, the exponential voltage recovery time constant τ_{pf} can be determined by

$$\tau_{pf} = -T/2 \Big/ \ln\left(\frac{V_{cap}(T/2) - V_{capSSpf}}{V_{capssf} - V_{capSSpf}}\right) \tag{5-22}$$

where the capacitor voltage after a half power frequency cycle is determined with (5-4), (5-5), and (5-7). The exponential voltage rise, compared to the actual capacitor voltage and absolute value of system voltage, can be seen in Figure 5.10. Time constant τ_{pf} is approximately 0.02sec.

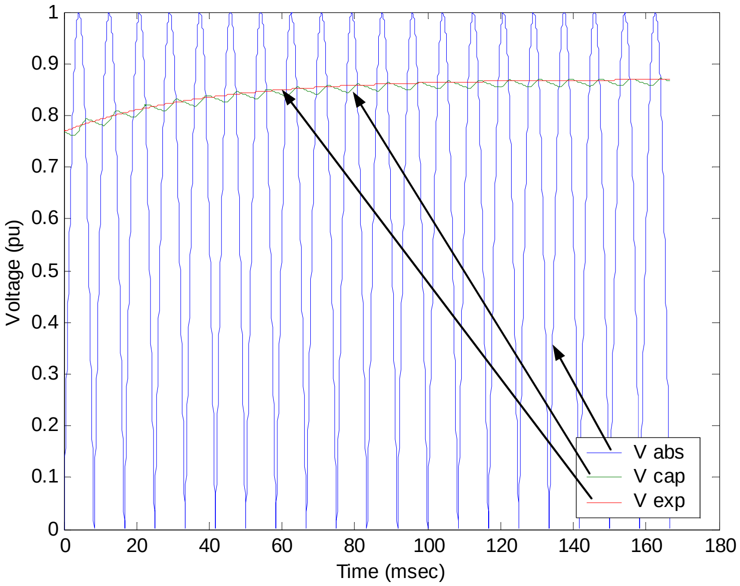


Figure 5.10. Exponential load capacitor voltage rise after the fault is cleared.

As the capacitor charges back to the pre-fault steady state voltage, the post-fault power decays back as an exponential PDF with the same time constant to the steady state power as seen in Figure 5.9. Referred to a DC system, the post-fault power response would be approximately

$$P(t) = V_{peak} \cdot \frac{(V_{peak} - V_{cap}(t))}{R} \tag{5-23}$$

where V_{peak} is the effective system voltage and R is the line resistance.

The energy necessary to recharge the capacitors back to steady state after the fault is cleared is shown by the shaded region E_2 in Figure 5.11. This region is equal to

$$E_2 = \int_{T_{pf}}^{t \to \infty} \left((P_1 - P_0) \exp\left(-\frac{t - T_{pf}}{\tau_{pf}} \right) \right) dt \tag{5-24}$$

which reduces to

$$E_2 = (P_1 - P_0) \cdot \tau_{pf} . \tag{5-25}$$

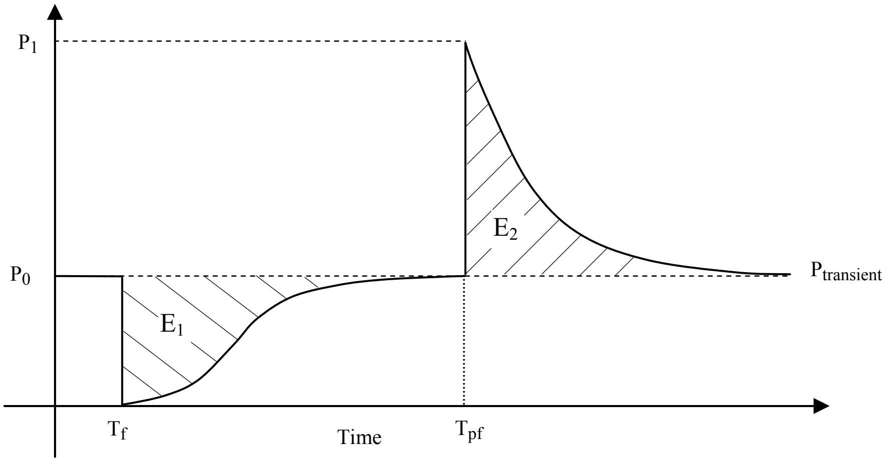


Figure 5.11. Energy dissipated E_1 and recovered E_2 by DC load capacitor.

The additional energy E_2 is equal to the energy dissipated by the capacitors during the fault. Avoiding the actual power electronic load dynamics, one can use the load recovery during the fault to calculate the amount of energy dissipated. The energy dissipated, shown by the shaded region E_1 in Figure 5.11, is equal to

$$E_1 = \int_{T_f}^{T_{pf}} \left(P_0 - P_f(t) \right) dt \le \frac{1}{2} C \cdot V_{capSSpf}^2 \tag{5-26}$$

which has an upper bound when the DC capacitor is completely discharged. The upper bound would be reached if the load capacitor voltage were to decay to zero before the fault clears (i.e., $\mu < T_{pf} - T_f$). If the load shuts-down at a certain capacitor voltage V_{trip}, the energy discharged would be limited further to

$$E_1 \leq \frac{1}{2} C \cdot \left(V_{capSSpf}^2 - V_{trip}^2 \right). \tag{5-27}$$

The energy discharged during the fault can alternatively be calculated knowing the capacitor voltage when the fault clears by

$$E_1 = \frac{1}{2} C \cdot \left(V_{capSSpf}^2 - V_{cap}^2 \left(T_{pf} \right) \right). \tag{5-28}$$

The power electronic dynamic equations are required to determine the capacitor voltage. Thus, E$_1$ is found with (5-26) or (5-27). Knowing E$_1$ = E$_2$, one can solve for the initial increase in power at fault clearing using (5-25) by

$$\left(P_1 - P_0 \right) = \frac{E_2}{\tau_{pf}} = \frac{E_1}{\tau_{pf}}. \tag{5-29}$$

The post-fault transient model characteristics are determined knowing the energy dissipated during the fault and the exponential voltage rise time constant. The power electronic transient post-fault model is an exponential PDF starting when the fault is cleared (T_{pf}) and is described as

$$P_{pf}\left(t \right) = P_0 + \frac{E_1}{\tau_{pf}} \cdot \exp\left(-\frac{t - T_{pf}}{\tau_{pf}} \right). \tag{5-30}$$

5.3 SUMMARY

The composite power electronic load recovers as a Weibull CDF in the fault and as an Exponential PDF after the fault is cleared. Beginning at the onset of the fault, the load transient response is

$$P_f\left(t \right) = P_{onset} + \left(P_0 - P_{onset} \right) \cdot \left(1 - \exp\left(-\left(\frac{t - T_f}{\lambda} \right)^k \right) \right) \tag{5-31}$$

when the system voltage is above the load shut-down setting, or else $P_f\left(t \right) = 0$. At fault clearing, the load transient response is

$$P_{pf}\left(t \right) = P_0 + \frac{E_1}{\tau_{pf}} \cdot \exp\left(-\frac{t - T_{pf}}{\tau_{pf}} \right). \tag{5-32}$$

Knowing the power electronic load model parameters P_0, R, L, C, and the voltage sag, the analytical dynamic equations (5-4), (5-5), and (5-7) along with the techniques in this chapter can be used to solve the composite transient model variables:

- onset power P_{onset},
- fault time constant λ,
- fault shape k, and
- post-fault time constant τ_{pf}.

In addition to the previous variables, the following variables are defined when running a simulation with the transient power electronic load model:

- onset time of fault T_f,
- clearing time of fault T_{pf}
- nominal power P_0
- load shut-down voltage V_{trip}, and
- DC capacitor energy dissipated in the fault E_1.

The energy dissipated is determined based upon the fault response and whether the load shuts-down.

Appropriate values for the transient model variables are determined in Chapter 6.

Chapter 6 – Power Electronic Transient Load Model Characteristics from Simulated Model Response

The power electronic transient load model characteristics are influenced by the model parameters R, L, C, P, and the voltage sag depth. This chapter determines the transient load model characteristics for 3125 cases in which the load parameters and voltage sag are varied. The objective is to determine trends in the characteristics to provide transient load models without direct solutions to the equations in Chapter 5.

6.1 TIME CONSTANTS AND SCALE FACTORS

The power electronic load transient response time constants τ_f and τ_{pf} are related to the RC time constant in a DC circuit. Since the applied voltage is not DC and the line impedance is not purely resistive, modifications are made. The exponential time constants of the power electronic load are

$$\tau_f = \tau_{base} \cdot \tau_{fscale} \text{, and} \tag{6-1}$$

$$\tau_{pf} = \tau_{base} \cdot \tau_{pfscale} . \tag{6-2}$$

As shown in section 6.2, based upon simulations a reasonable choice for τ_{base} is made by defining $\tau_{base} = |Z_{line}| \cdot C$ where $|Z_{line}|$ is the magnitude of line impedance and C is the equivalent load capacitance. Variables τ_{fscale} and $\tau_{pfscale}$ are time constant scale factors applied to τ_{base} to convert to a 60Hz load response time constant.

The reason for the scale factors is that the load restores for a short interval each half-cycle occurring during the shaded region of Figure 6.1a. The remaining part of the half-cycle the load capacitor is discharging. During the onset of a fault, when the capacitor voltage is above the fault steady state voltage, the load is discharging for the majority of the cycle. At fault clearing, the load is restoring for the majority of the cycle.

Figure 6.1a illustrates the capacitor restoring at fault clearing. The final voltage is greater than the initial voltage. To determine how τ_{base} is scaled over the complete half-cycle, the AC capacitor charging is referred to a DC circuit (Figure 6.1b). The capacitor charging period is indicated by volt-sec (*VS*) whose area is equal to

$$VS = \int_{T_1}^{T_2} \left(V_p \sin(\omega \cdot t) - V_{cap}(t) \right) dt \,. \tag{6-3}$$

Referred to a DC circuit, the average voltage ΔV is applied for the length of time $T_3 = \frac{VS}{\Delta V}$. The post-fault scale factor is approximately $\tau_{pfscale} = \frac{1/f/2}{T_3}$. When $V_{cap} \to 0$, $\Delta V \to V_p$, $T_1 \to 0$, and $T_2 \to \pi$, $\tau_{pfscale}$ is approximately 1.57 (i.e., π/2). The *RLC* load model parameters, size of the total power electronic load, and the depth of the voltage sag all influence the time constant scale factors.

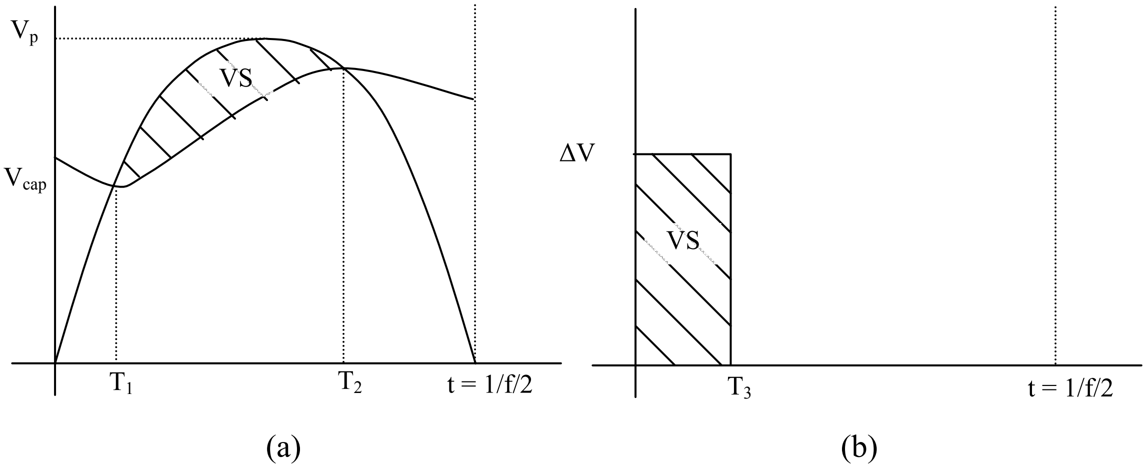


Figure 6.1. Post-fault capacitor charging (a) on the AC system and (b) referred to a DC equivalent circuit.

In the following two sections, I determine how the time constants and scale factors vary for 3125 different cases using the technique from Chapter 5 and varying the model parameters *R*, *L*, *C*, *P*, and voltage sag depth. The model parameters I used are:

- C = {2000, 4000, 6000, 8000, 10000}uF
- R = {2, 4, 6, 8, 10}ohm
- L = {2, 4, 6, 8, 10}mH
- P = {300, 700, 1100, 1500, 1900}W
- Voltage Sag = {0.55, 0.65, 0.75, 0.85, 0.95}pu on 208Vrms

6.2 POST-FAULT TIME CONSTANTS

For the five values of *R*, *L*, *C*, *P*, and voltage sag, I calculate the post-fault time constants using the technique developed in Chapter 5. The post-fault time constants τ_{pf} for the 3125 events can be seen in Figure 6.2. The model parameters and sag depth have a significant impact on τ_{pf}. The range is between 0.01 and 0.3sec.

The post-fault scale factors are then determined using (6-2). The post-fault scale factors $\tau_{pfscale}$ vs. $\tau_{base} = |Z_{line}| \cdot C$ can be seen in Figure 6.3. Scale factor $\tau_{pfscale}$ varies between 1 and 4. If an *RC* base time constant had been used, the variation in $\tau_{pfscale}$ increases to the range of 1 to 8. Scale factor $\tau_{pfscale}$ correlates best for the $|Z_{line}| \cdot C$ base time constant.

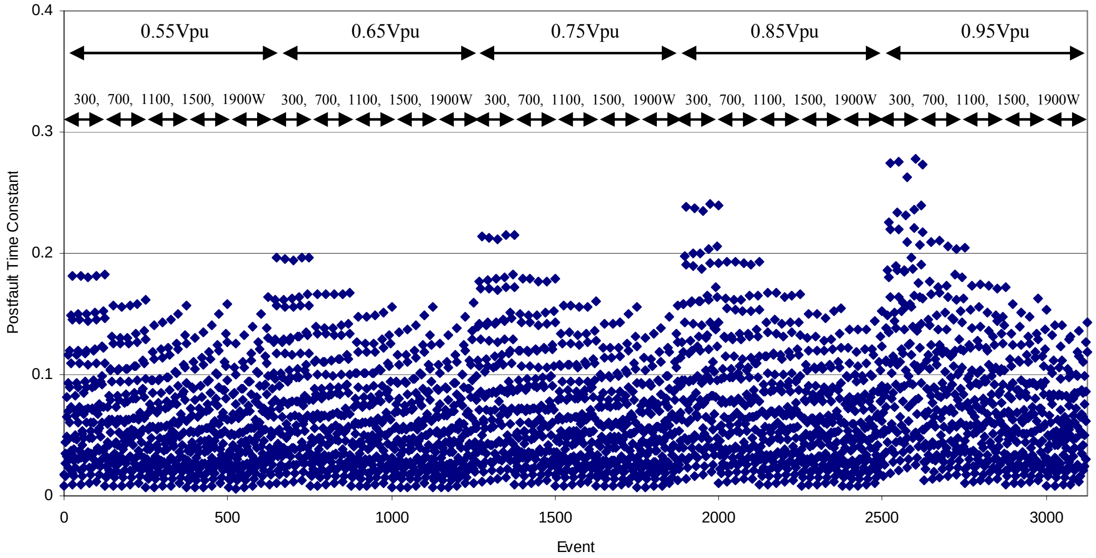


Figure 6.2. Time constant τ_{pf} for all varied load model parameters and voltage sags.

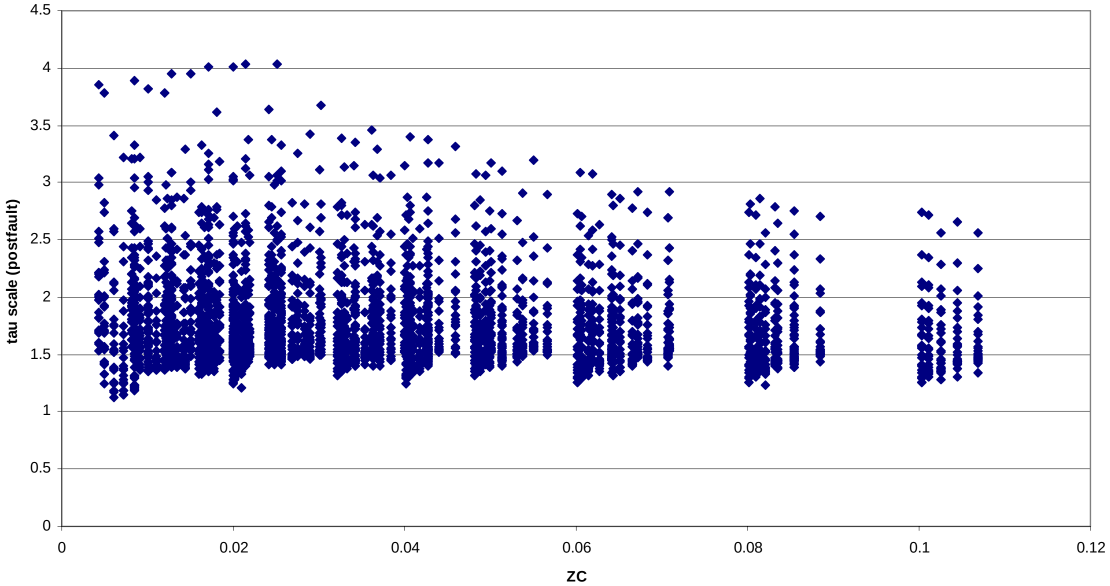


Figure 6.3. Scale factor $\tau_{pfscale}$ vs. base time constant $\tau_{base} = |Z_{line}| \cdot C$.

Figure 6.4 shows the most influential model parameters on $\tau_{pfscale}$ for all 3125 events. The varied parameters are ordered by capacitance, resistance, inductance, power, and fault voltage. Each parameter increases when varied and are varied by five layered loops. The arrows above the plot show the varied parameters.

Low fault voltage results in a lower steady state capacitor voltage and therefore longer restoring intervals at fault clearing. These situations reduce $\tau_{pfscale}$. The increase in load also decreases the steady state capacitor voltage and reduces $\tau_{pfscale}$ to approximately 1.5. The most influential parameter to $\tau_{pfscale}$ is the voltage sag depth followed by the size of the load. Only for shallow faults lightly loaded with power electronics does $\tau_{pfscale}$ increase significantly.

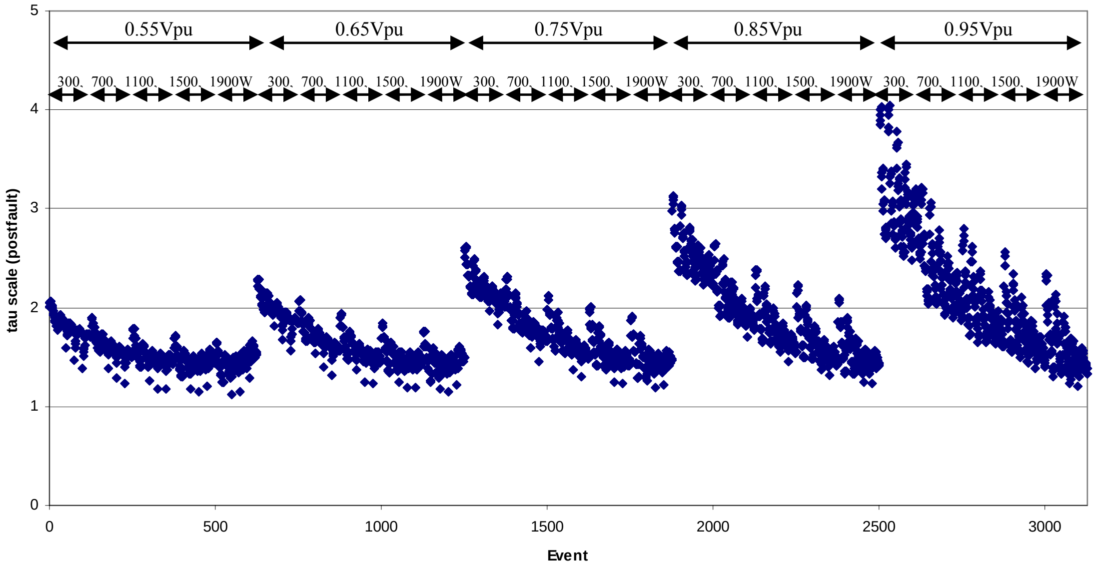


Figure 6.4. Scale factor $\tau_{pfscale}$ for all 3125 case events.

In Figure 6.5, the fault voltage is 0.75pu for all events. The increase in load shows a noticeable decrease $\tau_{pfscale}$. As the system inductance increases, the duration of the restoring intervals increase to allow power transfer which results in a lower steady state capacitor voltage. The reduced capacitor voltage leads to longer restoring intervals at fault clearing and a lower $\tau_{pfscale}$.

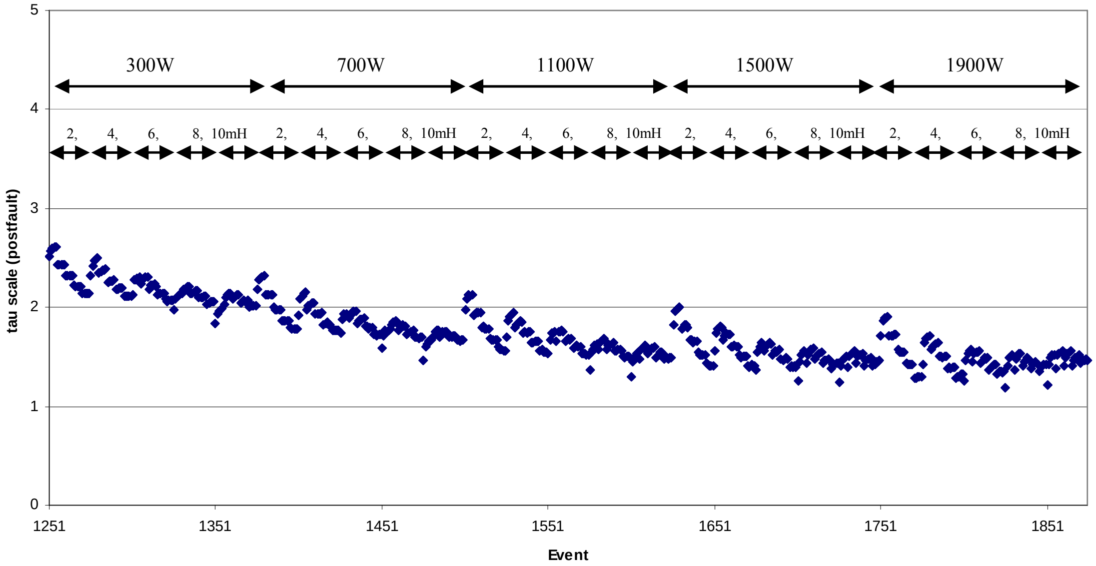


Figure 6.5. Scale factor $\tau_{pfscale}$ for events with 25% voltage sag and RLC and P varied.

In Figure 6.6, the fault voltage is 0.75pu and the power electronic load is 1100W for all events. The increase in inductance causes $\tau_{pfscale}$ to converge near 1.5. The increase in resistance increases the voltage drop to the capacitor and results in a lower steady state capacitor voltage. The lower capacitor voltage leads to longer restoring intervals at fault clearing and a lower $\tau_{pfscale}$.

Every five points, the load capacitance increases and then repeats. The change in capacitance has a slight yet varied affect on $\tau_{pfscale}$. The capacitance has a more significant affect on the loads storage factor and therefore overall time constant.

If the system impedance and capacitance are known, $\tau_{pfscale} = 1.5$ can be used to approximate τ_{pf}. Typically, for composite loads, however, the system and load parameters are unknown and must be estimated using common design specifications for the power electronic load.

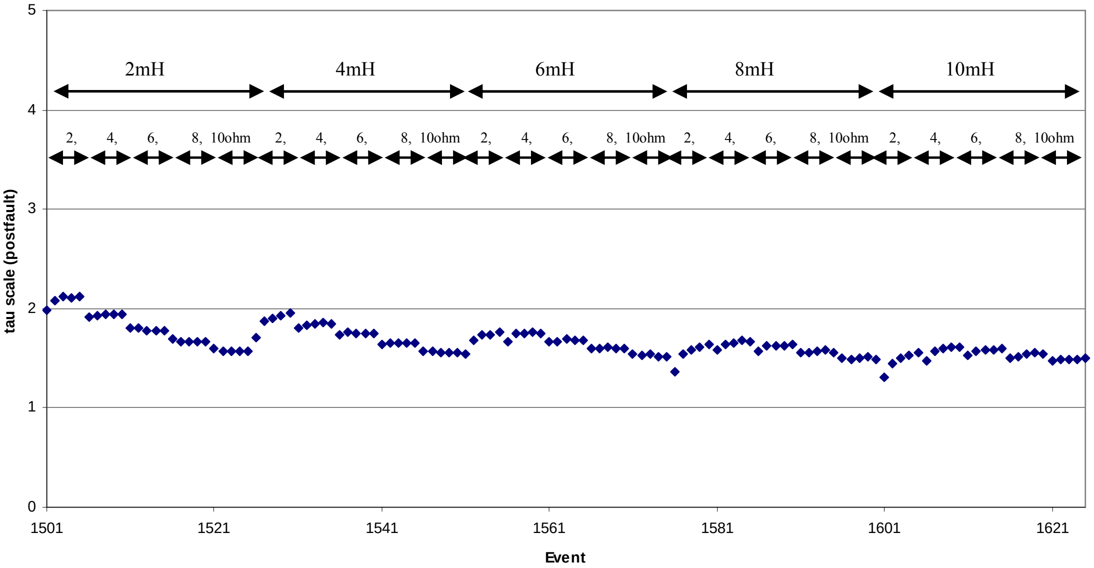


Figure 6.6. Scale factor $\tau_{pfscale}$ for events with 25% voltage sag, 1100W load, and RLC varied.

Power electronic loads are commonly designed for 5% voltage ripple. At 208V, the approximate storage factor β = 1uF/W. In Figure 6.7, τ_{pf} is shown for events with a 0.5-1.5uF/W storage factor. In these events, the range in τ_{pf} is greatly reduced. The time constants, greater than 0.04sec, are due to large loads with high line impedance. With a set storage factor, large loads result in high capacitance. Therefore, associated with high line impedance, the time constants increase. However, as the size of the composite load increases, the parallel load impedance will decrease. The typical average post-fault time constant is slightly larger than one power frequency cycle (i.e., 0.02sec).

Scale factor $\tau_{pfscale}$ for these events are near 1.5 and can be seen in Figure 6.8. The overall post-fault time constant is best determined using

$$\tau_{pf} = 1.5 \cdot |Z_{line}| \cdot \beta \cdot 2P_{load} . \tag{6-4}$$

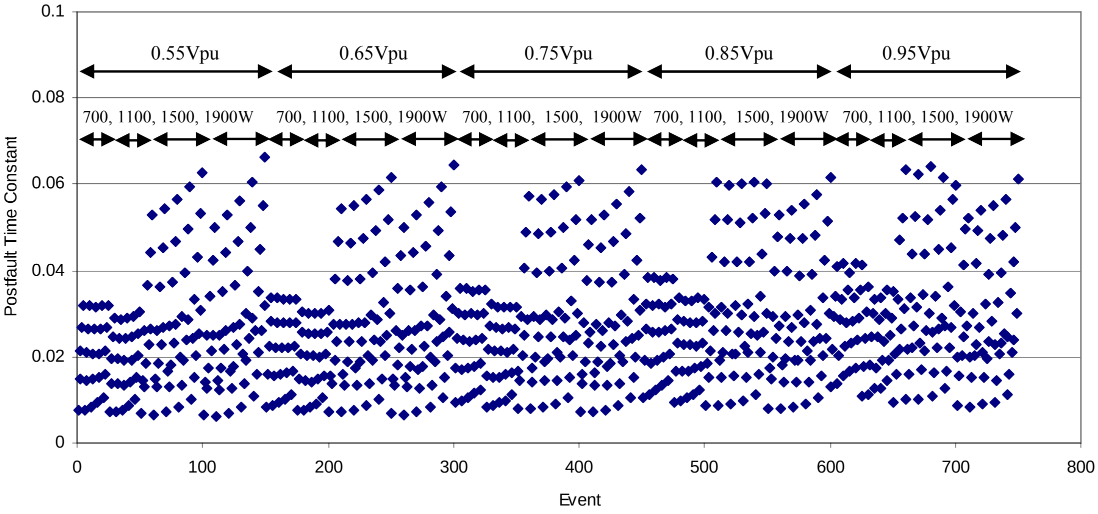


Figure 6.7. Time constant τ_{pf} for events with storage factor permitting 5% voltage ripple.

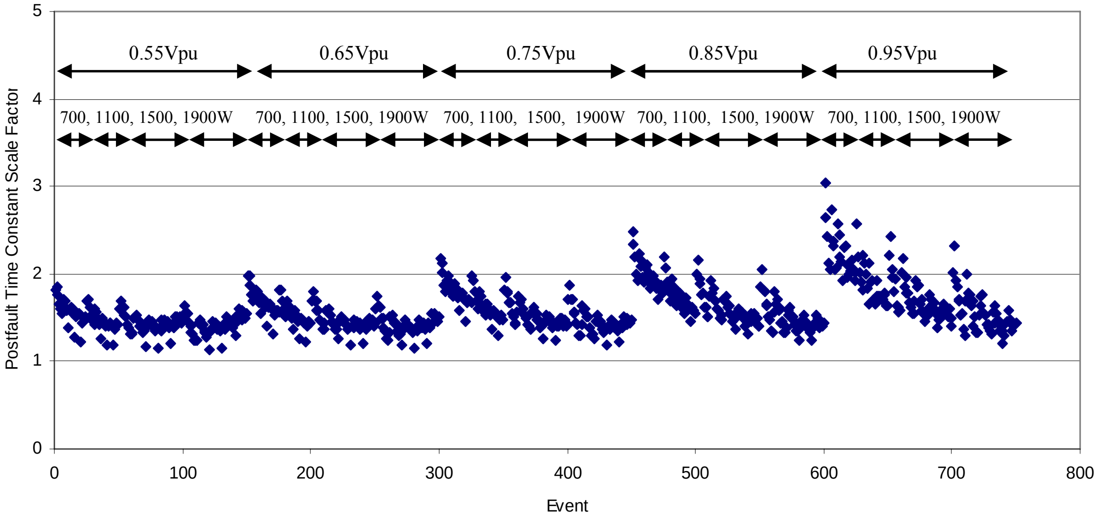


Figure 6.8. Scale factor $\tau_{pfscale}$ for events with storage factor permitting 5% voltage ripple.

6.3 FAULT TIME CONSTANTS

The exponential fault time constant τ_f is variable with system parameters as shown in Figure 6.9. Scale factor τ_{fscale} correlates best to $\tau_{base} = |Z_{line}| \cdot C$.

In Figure 6.10, one can see the change in τ_{fscale} due to the change in the varied parameters and voltage sag. Although τ_{fscale} converges near 1.5, the range in τ_{fscale} is greater than $\tau_{pfscale}$. This occurs because the load capacitor discharges slower during the fault due to its storage factor than the load capacitor can restore after the fault is cleared. The fault scale factor τ_{fscale} has an average value approximately equal to three. The approximate fault time constant τ_f is

$$\tau_f = 3 \cdot |Z_{line}| \cdot \beta \cdot 2P_{load} \,. \tag{6-5}$$

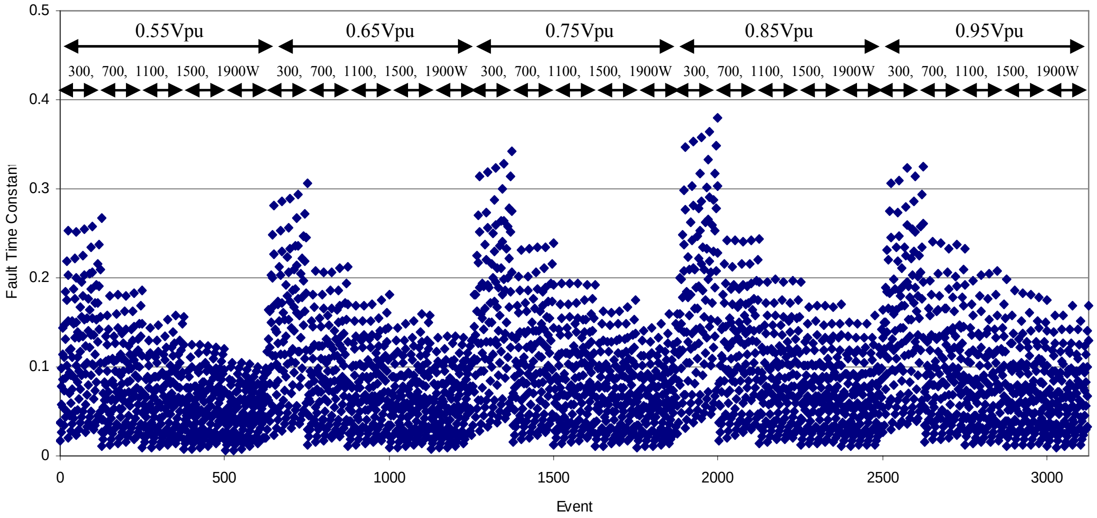


Figure 6.9. Time constant τ_f for all varied load model parameters and voltage sags.

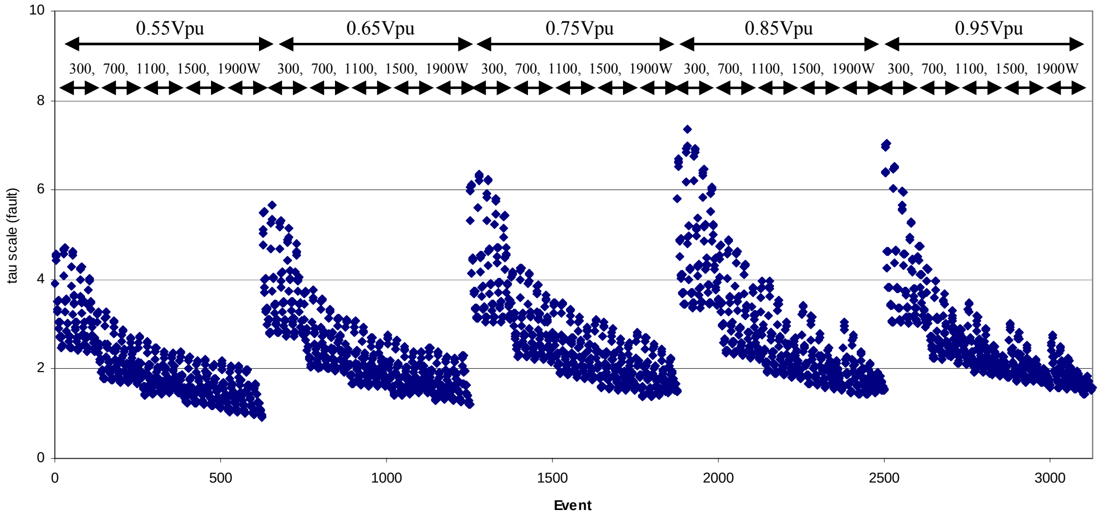


Figure 6.10. Scale factor τ_{fscale} for all 3125 case events.

Solving the ride-through time μ using the steady state pre-fault and peak fault voltage, I determined the Weibull time constant λ and shape k which are given in Figure 6.11 and 6.12, respectively. When $\mu \leq 0$, $k = 1$ (exponential) and $\lambda = \tau_f$ with an onset power. Ride-through μ increases for large storage factors and even further for deep voltage sags. As μ increases greater than zero, the shape increases from one and λ increases greater than τ_f because λ includes the ride-through time. Time constant λ greater than 0.1sec is due to high storage factors causing a long ride-through.

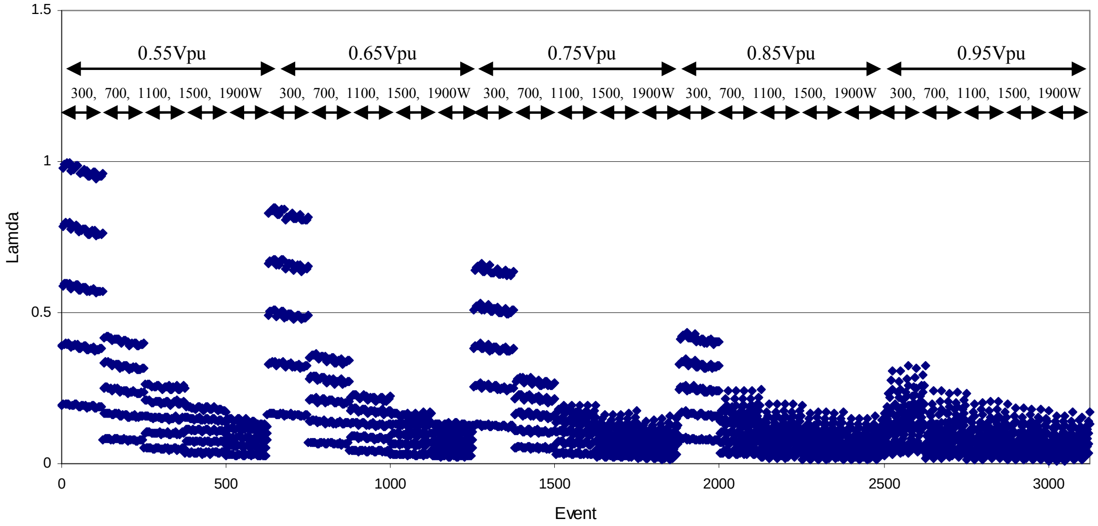


Figure 6.11. Weibull time constant λ for all 3125 case events.

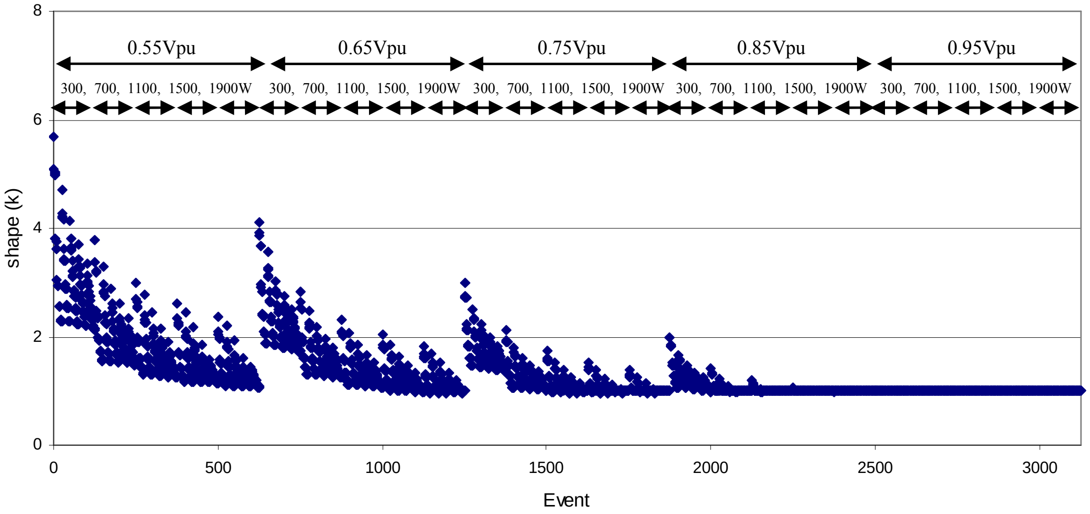


Figure 6.12. Weibull shape factor *k* for all 3125 events.

In Figure 6.13, the Weibull time constants are shown for events having a storage factor allowing approximately 5% voltage ripple. The set storage factor limits the ride-through time μ by

$$\mu = \left(V_{capSSpf}^{2} - V_{peakf}^{2}\right) \cdot \beta \,. \tag{6-6}$$

In the events where there is no ride-through time ($\mu \leq 0$), the shape (shown in Figure 6.14) is one and $\lambda = \tau_f$. For deeper voltage sags where there is ride-through time ($\mu > 0$), the shape is greater than one and λ is approximately $\mu + \tau_f$. Time constant λ is relatively constant because μ is a small number, and when μ increases, τ_f decreases due to the decrease in τ_{fscale} for deep voltage sags as shown in Figure 6.10. For the set storage factor allowing 5% voltage ripple, λ is approximately 0.04sec and $k \approx 1.1$.

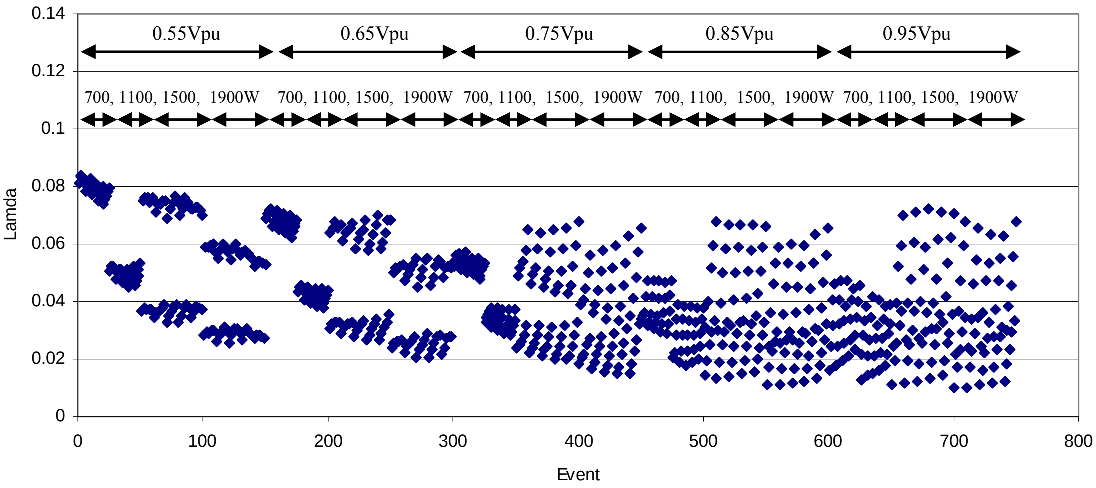


Figure 6.13. Weibull time constant λ for events with set storage factor.

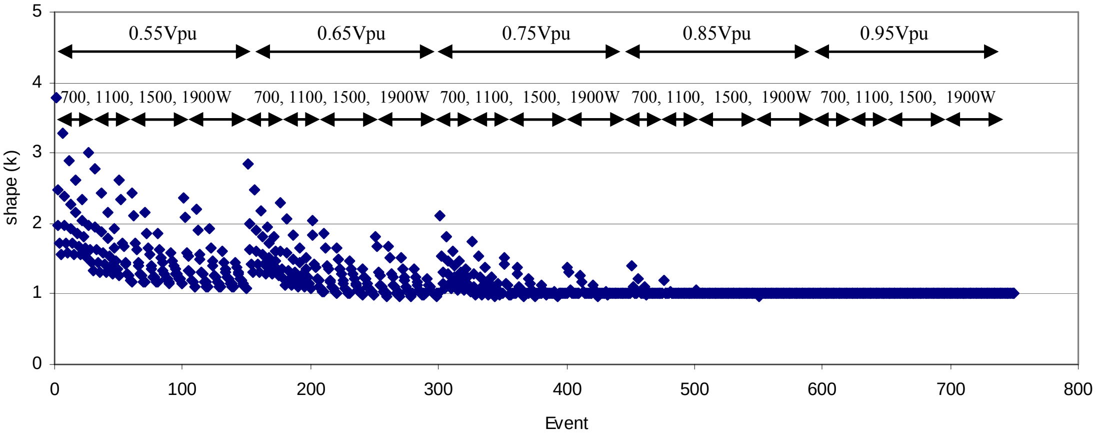


Figure 6.14. Weibull shape factor *k* for events in Figure 6.13.

6.4 SUMMARY

The Weibull shape of the fault load recovery is dependent primarily on voltage sag depth. The shape increases from one as the sag depth increases. For large loads, however, the fault shape is always approximately one (exponential). When the shape is one, $\lambda = \tau_f$, and τ_f can be estimated as $\tau_f = 3 \cdot |Z_{line}| \cdot \beta \cdot 2P_{load}$.

The post-fault time constant τ_{pf} can be estimated as $\tau_{pf} = 1.5 \cdot |Z_{line}| \cdot \beta \cdot 2P_{load}$. The scale factor converges to 1.5 for large loads and deep voltage sags. The post-fault time constant is approximately half the fault time constant because the capacitor voltage restores faster after the fault than the capacitor voltage decays during the fault. This is due to the storage factor of the load.

Summarizing the findings of this chapter, the recommendations for modeling the average power electronic load are:

- $\lambda = 0.04$sec,
- $k = 1.1$, and
- $P_{onset} = 0$.
- $\tau_{pf} = 0.02$sec.

Chapter 7 – Laboratory Power Electronic Load Response

The Voltage Sag-Test Station first used in Chapter 3 to test the response of linear loads, has been modified to test the transient response of power electronic loads. The actual response from controlled power electronic loads is compared to the transient model whose characteristics are determined using the technique described in Chapter 5.

Commonly, power electronic loads have a step-down transformer and regulate 12 and/or 5Vdc to the electronic components. Commercial products would work as test loads; however, *RLC* and *P* are not adjustable. For my tests, I have constructed several loads consisting of a step-down transformer, diode bridge rectifier (DBR), and boost converter equipped with proportional/integral (PI) control to regulate the output voltage. The design provides a constant DC output voltage which is necessary for a constant power load. The boost converter doubles the load voltage to 90Vdc so standard incandescent light bulbs can be used to draw power. The schematic for one power electronic load is shown in Figure 7.1.

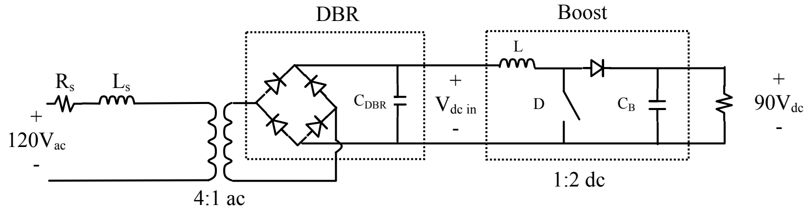


Figure 7.1. Power electronic load schematic with boost converter.

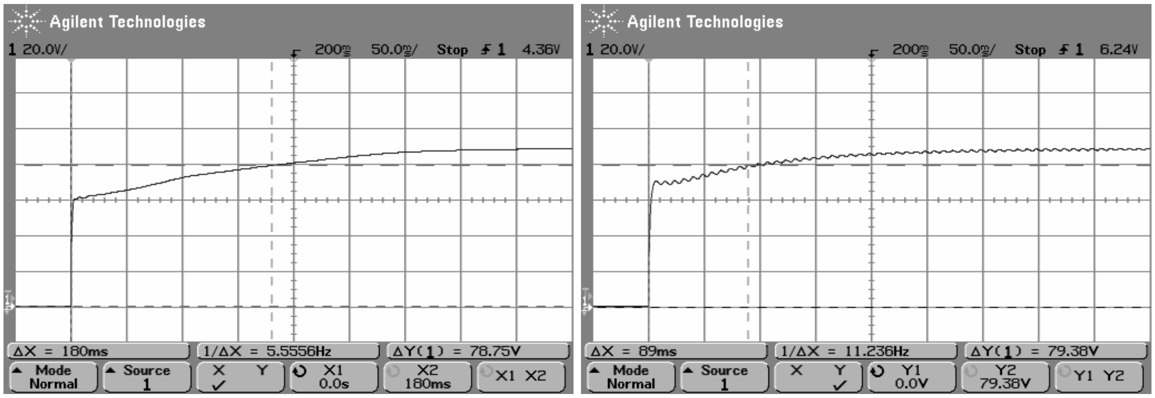
7.1 COMPOSITE POWER ELECTRONIC LOAD MODEL PARAMETERS

7.1.1 Equivalent Capacitance

The DBR capacitor in parallel with the boost converter capacitor affects the total capacitance and therefore storage factor and time constants of the power electronic load. The capacitance of the boost converter is reflected back to the DBR circuit according to the steady state duty cycle *D* of the boost converter firing circuit. The longer the duty cycle, the longer the boost output is disconnected from the boost input. During *1-D*, the boost capacitor is in parallel with the DBR capacitor. The circuit time constants change due to the duty cycle. The bump test energizing time constant in Figure 7.2a is due to a 40% duty cycle while Figure 7.2b represents a 60% duty cycle. The time constant in Figure 7.2a is slightly longer meaning more capacitance is reflected back to the DBR increasing the total load capacitance. The equivalent capacitance referred to the source is approximately

$$C_{eq} = \frac{(1/n_1)^2 \cdot C_B(1-D) + C_{DBR}}{{n_2}^2} \tag{7-1}$$

where C_B is the boost converter capacitance and C_{DBR} is the DBR capacitance. The boost converter acts like a step-up transformer with $n_1 = ½$, the source step-down transformer has $n_2 = 4$, and the duty cycle $D \approx 0.5$.



(a) (b)

Figure 7.2. Time constant due to (a) 40% duty cycle and (b) 60% duty cycle.

7.1.2 System Impedance

The system impedance consists of the source and load transformer series impedances. To measure the system impedance, I use the Passive Agent System Impedance Monitoring Station (PASIMS) [23] explained thoroughly in Appendix D. The station uses the power electronic load current pulse and associated voltage drop to directly measure and also interpolate the power frequency system impedance. The setup is shown in Figure 7.3.

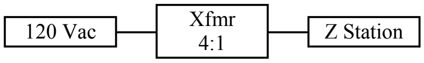


Figure 7.3. Setup to measure system impedance.

With PASIMS I found the impedance for the system and the two transformers used in the power electronic loads. The 120V system impedance is shown in Table 7.1 for the three configurations:

- System (no transformer)
- System and large 4:1 transformer
- System and small 4:1 transformer

Table 7.1. System Impedance Referred to 120V.

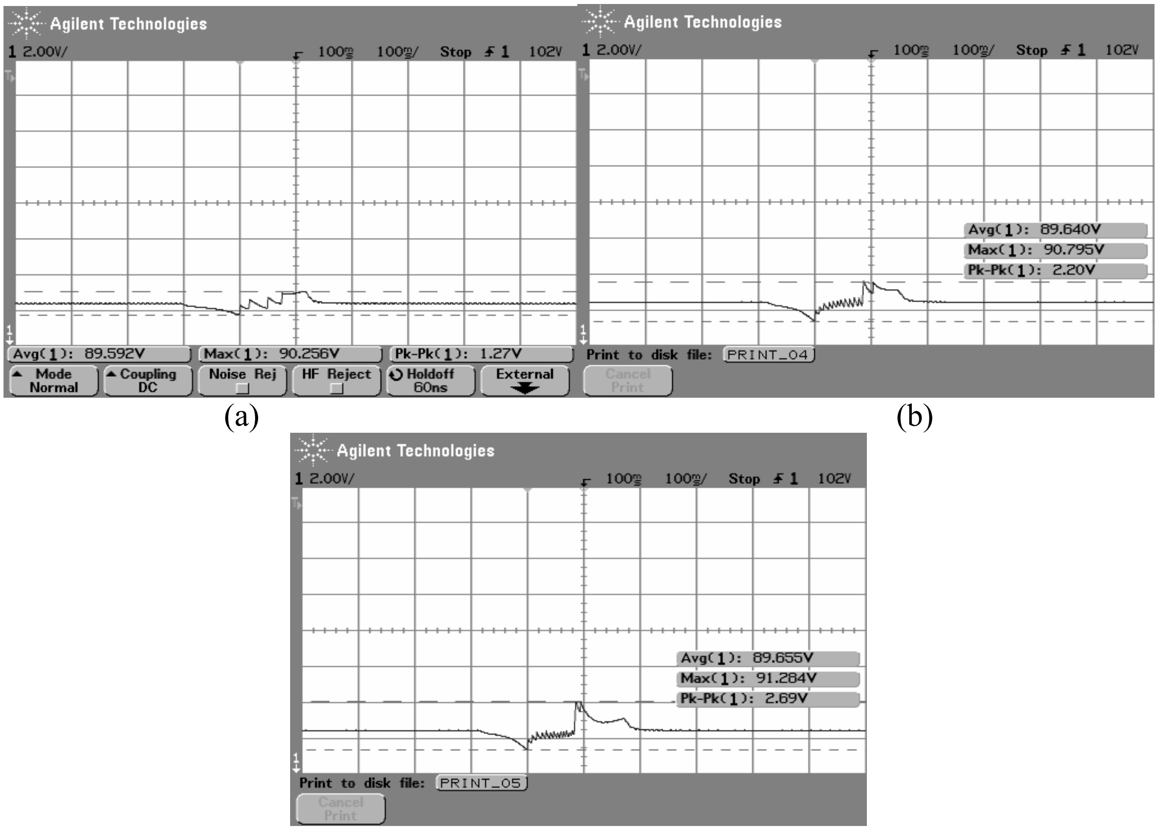
	System	Large 4:1 xfmr	Small 4:1 xfmr
R (ohm)	0.31	10.25	2
L (mH)	0.03	8	9

7.1.3 Proportional/Integral Control

The schematic for the proportional/integral (PI) feedback control and firing circuit is shown in Appendix E. The controller adjusts the duty cycle of the Boost circuit during the fault to maintain a constant output voltage to the resistive load. This creates a constant power load. The PI controller compares a scaled-down value of the output voltage to the user 'Voltage Set Point.' Under steady state conditions, the difference is zero and the duty cycle is constant. During an event however, the difference increases and the PI controller adjusts the duty cycle driving the difference back to zero. The PI controller can be tuned to optimize the response [24].

Integral control has a fast response while proportional control is slower. The optimal response was found with low integral (1/8 turn) and high proportional (5/6 turn) gain. The response for 10%, 20%, and 30% ten cycle voltage sags where the load is 60W and the equivalent capacitance is 1500uF can be seen in the Figures 7.4a, 7.4b, and 7.4c, respectively.

During each of the voltage sags, the PI controller begins adjusting the duty cycle with proportional control. After approximately 100ms (6 cycles), integral control takes over which causes voltage ringing. The voltage overshoot occurring ten cycles after the onset of the fault is due to the system voltage recovery when the fault clears.



Avg(1): 89.592V
Max(1): 90.256V
Pk-Pk(1): 1.27V

(a)

Avg(1): 89.640V
Max(1): 90.795V
Pk-Pk(1): 2.20V

(b)

Avg(1): 89.655V
Max(1): 91.284V
Pk-Pk(1): 2.69V

(c)

Figure 7.4. Optimal control for (a) 10% sag, (b) 20% sag, (c) 30% sag with 60W load.

The voltage response for non-optimal PI control is illustrated in Figure 7.5 for a ten cycle 30% voltage sag with a 60W load and 1675uF equivalent capacitance. The control takes too long to correct the output voltage and results in a significant overshoot when the fault clears. As the voltage is decaying, the continued control overcorrects the voltage below the set-point. Inductance in the feedback line can also cause improper feedback control.

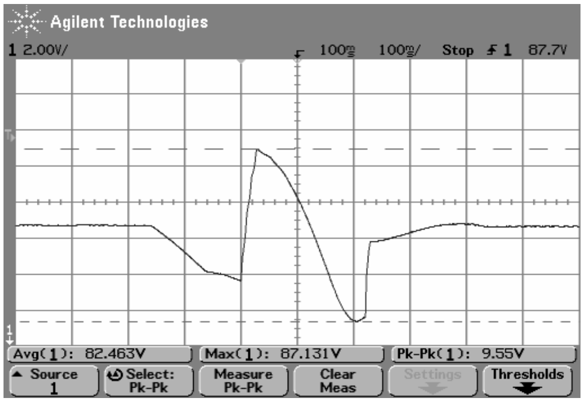


Figure 7.5. Non-optimal control for 30% sag with 60W load.

7.2 TEST USING SINGLE TRANSFORMER

In these tests, the individual and composite loads are served off a single step-down transformer. This causes the system impedance to be similar for the individual and composite loads. The test setup for the composite load served off the large transformer is shown in Figure 7.6. The diode represents the DBR and C is the equivalent DBR and boost converter capacitance.

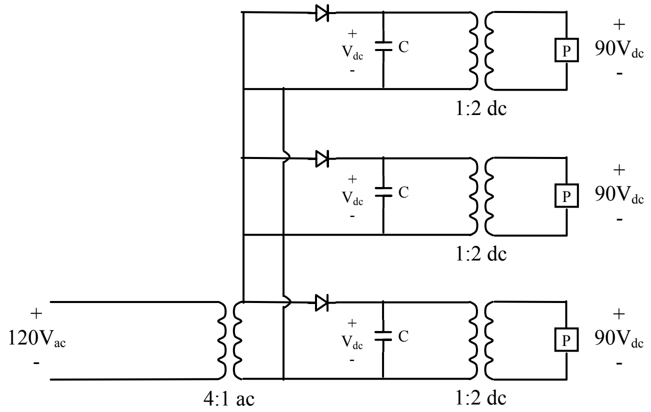


Figure 7.6. Test setup for composite power electronic load served from one transformer.

7.2.1 Same Capacitance, Different Power

The three individual loads are 86, 51, and 36W. Each load has an equivalent capacitance of 1500uF and experiences a ten cycle 20% voltage sag. The individual and composite load model parameters and transient characteristics determined using the technique from Chapter 5 are given in Table 7.2. Characteristics λ and *k* do not apply for the individual loads but have been included to show their composite distribution characteristics.

Table 7.2. Load Model Parameters and Transient Characteristics: Large Transformer Tests – Same Capacitance, Different Power

P (W)	Sag (Vpu)	C_{eq} (uF)	R (ohm)	L (mH)	$V_{capSSpf}$ (V)	V_{capSSf} (V)	μ (sec)	τ_f (sec)	τ_{fscale}	λ (sec)	k	τ_{pf} (sec)	$\tau_{pfscale}$
86	0.8	1500	10.25	8	148	114	0.030	0.054	3.363	0.090	1.272	0.035	2.160
51	0.8	1500	10.25	8	154	119	0.078	0.069	4.290	0.159	1.562	0.039	2.439
36	0.8	1500	10.25	8	157	122	0.130	0.079	4.946	0.226	1.808	0.042	2.611
184	0.8	4500	8	7	140	106	0.014	0.107	2.834	0.126	1.037	0.073	1.928

Figures 7.7, 7.8, and 7.9 show the actual average system power load response for the 86, 51, and 36W load, respectively. Due to a low pass filtering effect when using a sliding window to average the waveform, the initial power appears to increase and sudden transitions appear more gradual. As the size of the load decreases, the steady state capacitor voltage and ride-through time increases. The fault response is exponential after the load reconnects to the system.

The time constants τ_f and τ_{pf} are similar in each individual case because the system impedance and capacitance are the same. As the load increases, however, there is a slight decrease in time constants. This is because the steady state capacitor voltage decreases and results in decreased scale factors. Time constant τ_f has a scale factor of approximately 4 and τ_{pf} has a scale factor of approximately 2.5. The magnitude of the post-fault inrush varies due to the steady state power, discharged energy, and post-fault time constant.

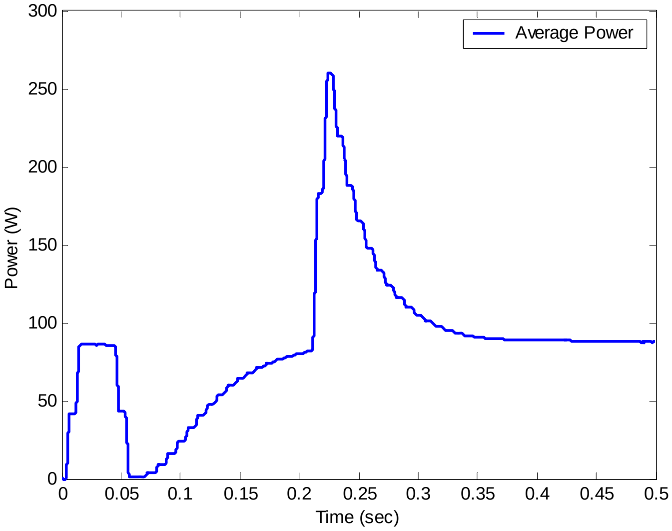


Figure 7.7. 86W actual individual power electronic load response.

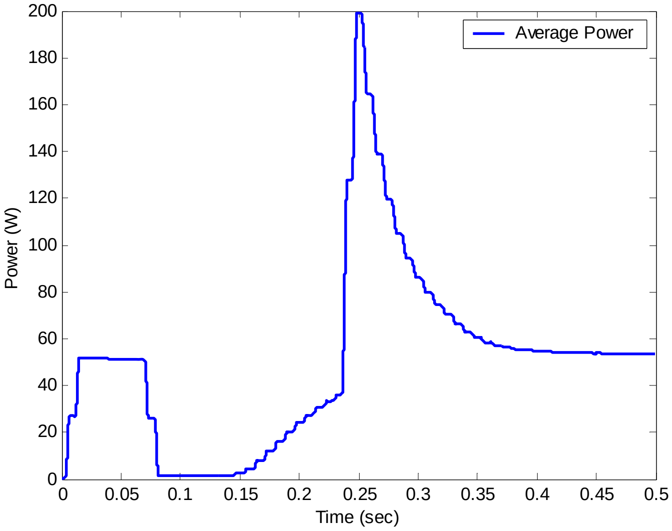


Figure 7.8. 51W actual individual power electronic load response.

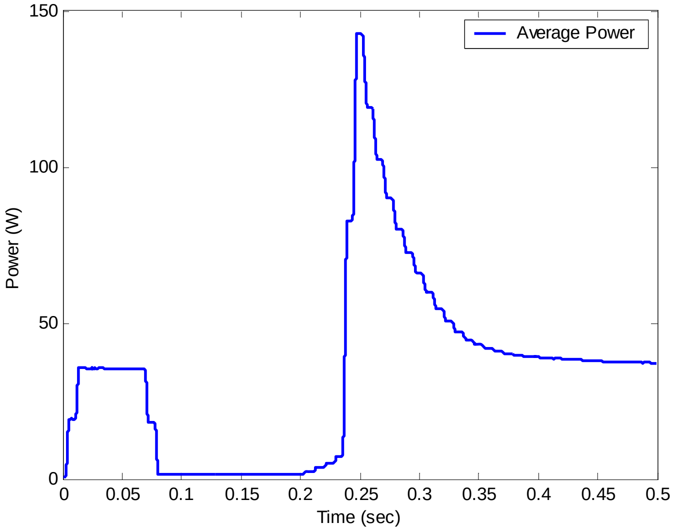


Figure 7.9. 36W actual individual power electronic load response.

Figure 7.10 shows the actual composite load transient response of the three individual loads above. The composite response is different from the individual load responses. The increased voltage drop across the single transformer decreases the steady state capacitor voltage at all three DBRs. The fault response shape is near exponential ($k = 1$) because the pre-fault steady state capacitor voltage is approximately the peak fault voltage.

The effective capacitance triples while the system impedance remains relatively constant. Time constant λ is approximately $\mu + \tau_f$, while τ_f is approximately $3\left|Z_{line}\right| \cdot C$ and μ is approximately zero. The post-fault time constant increases due to total load capacitance, however, $\tau_{pfscale}$ decreases to approximately 1.9 due to the increase in load.

The power electronic load transient characteristics are used to simulate the load response in Figure 7.11. These responses are similar.

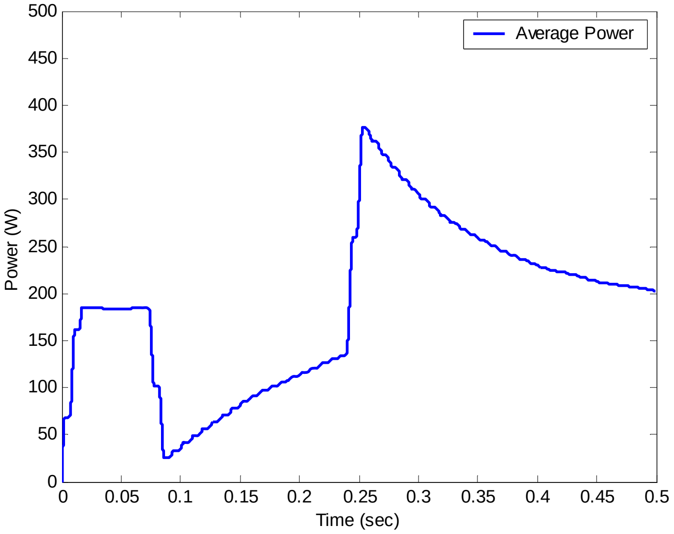


Figure 7.10. 184W actual composite power electronic load response.

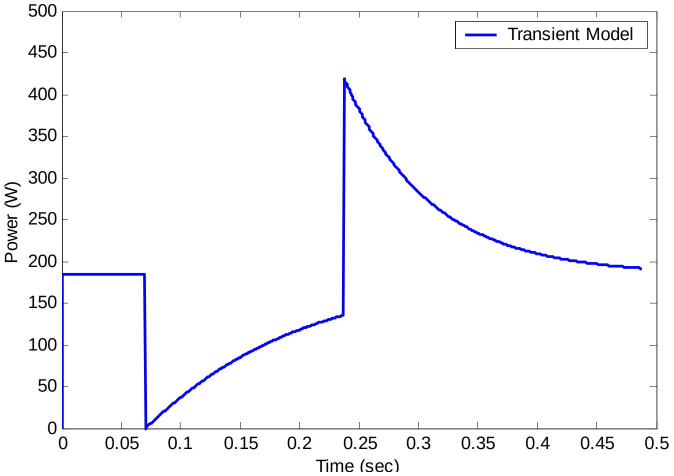


Figure 7.11. Power electronic load model response of Figure 7.10.

7.2.2 Same Power, Different Capacitance

Using the large transformer and an approximate 50W load for each test, the transient responses are acquired when varying the load capacitance. Each fault is a ten cycle 20% voltage sag. The parameters and determined characteristics for the individual and composite power electronic loads are given in Table 7.3. Characteristics λ and *k* do not apply for the individual loads but have been included to show their composite distribution characteristics.

Table 7.3. Load Model Parameters and Transient Characteristics: Large Transformer Tests – Same Power, Different Capacitance.

P (W)	Sag (Vpu)	C_{eq} (uF)	R (ohm)	L (mH)	$V_{capSSpf}$ (V)	V_{capSSf} (V)	μ (sec)	τ_f (sec)	τ_{fscale}	λ (sec)	k	τ_{pf} (sec)	$\tau_{pfscale}$
50	0.8	800	10.25	8	154	120	0.042	0.034	4.018	0.083	1.611	0.020	2.391
51	0.8	1500	10.25	8	154	119	0.078	0.069	4.290	0.159	1.562	0.039	2.439
48	0.8	2500	10.25	8	154	120	0.138	0.116	4.328	0.274	1.592	0.066	2.454
154	0.8	4800	8	7	143	109	0.031	0.122	3.010	0.161	1.108	0.082	2.028

Figures 7.12, 7.13, and 7.14 show the response of 50W loads with 800, 1500, and 2500uF equivalent capacitance, respectively. Each individual load rides-through part of the fault before reconnecting to the system. It is evident that the time constants and ride-through increase with the increase in capacitance. Time constant τ_f has a scale factor of approximately 4 and τ_{pf} has a scale factor of approximately 2.4.

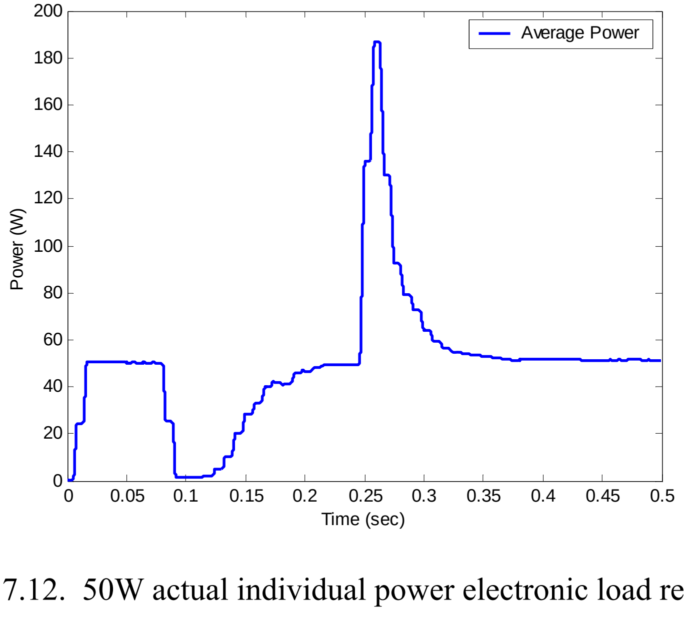


Figure 7.12. 50W actual individual power electronic load response.

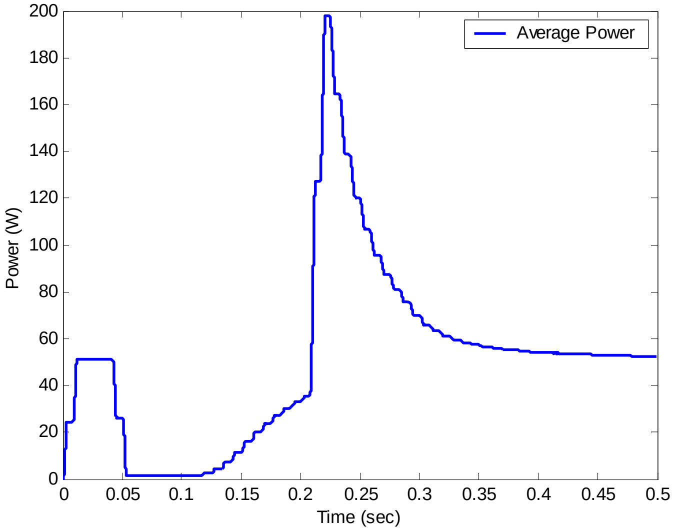


Figure 7.13. 51W actual individual power electronic load response.

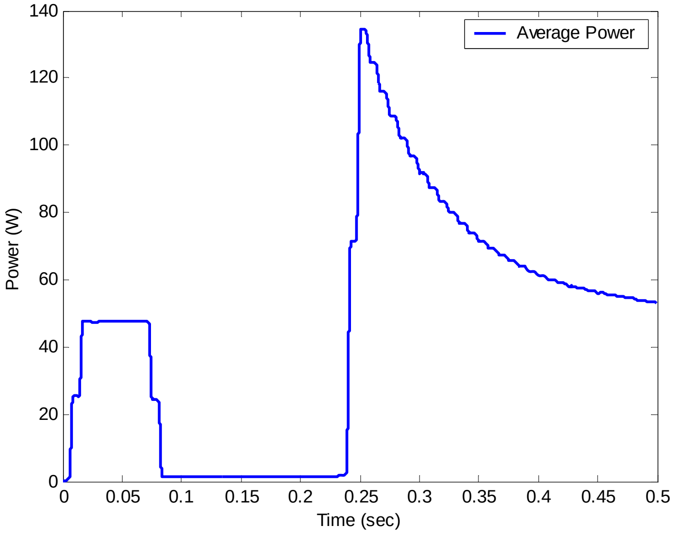


Figure 7.14. 48W actual individual power electronic load response.

The previous three loads are connected in parallel to form one composite load whose response to a similar fault can be seen in Figure 7.15. Due to the large voltage drop from the transformer impedance, all the power electronic load capacitors have a lower pre-fault steady state voltage. Therefore, the composite load fault response shape is near exponential and λ is approximately $\mu + \tau_f$, while τ_f is approximately $3|Z_{line}|\cdot C$ and μ is approximately zero. The post-fault time constant increases due to an increase in capacitance while the scale factor decreases due to the increase in load.

The transient power electronic load model with the characteristics from Table 7.3 is used to regenerate the actual composite load response. The model response is shown in Figure 7.16.

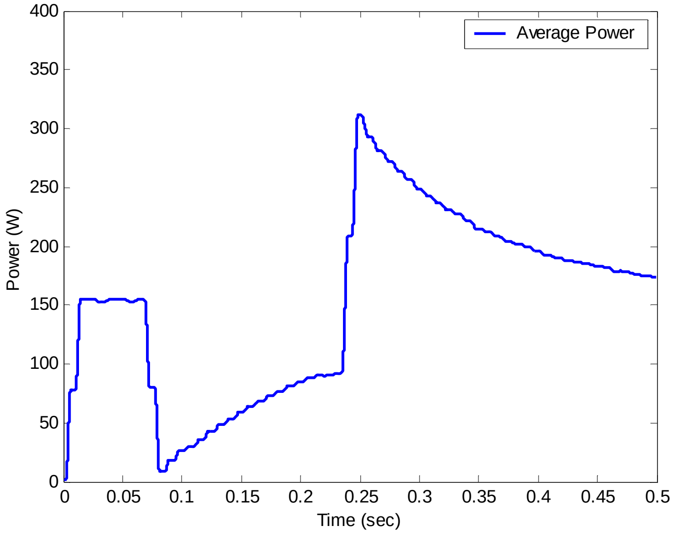


Figure 7.15. 154W actual composite power electronic load response.

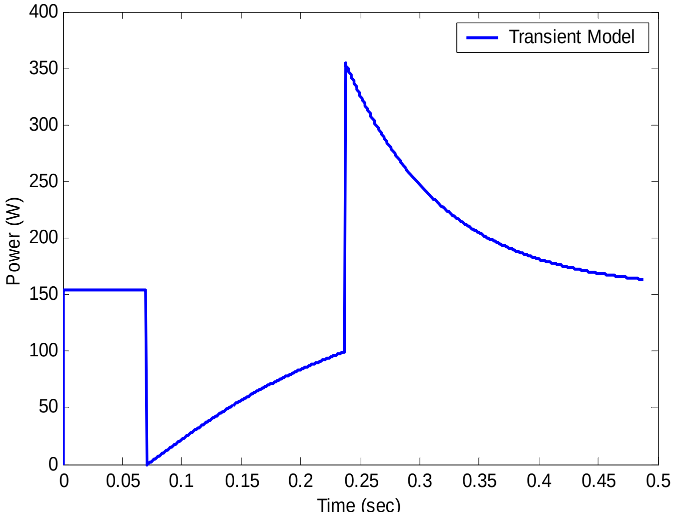


Figure 7.16. Power electronic load model response of Figure 7.15.

7.3 TEST USING THREE TRANSFORMERS

In these tests, separate transformers are used for each power electronic load. The composite load test setup is shown in Figure 7.17.

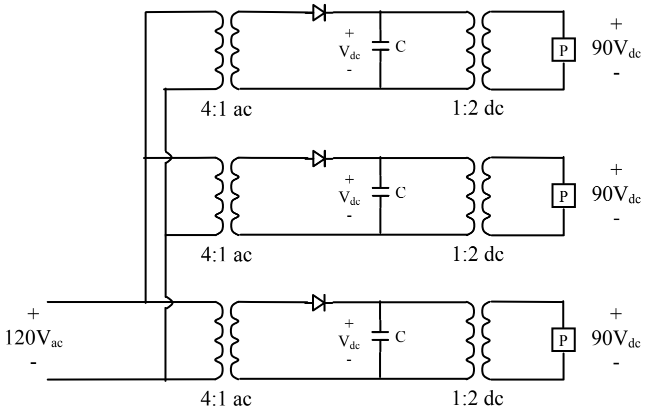


Figure 7.17. Test setup for three power electronic loads served from separate transformers.

As a composite load, the voltage drop across each transformer will be independent from the other loads. Therefore, the composite load responds as the sum of the individual responses. Figure 7.18a shows an example of the actual composite power electronic load response with three isolated loads with different storage factors. Figure 7.18b shows the transient load model response for the composite load in Figure 7.18a.

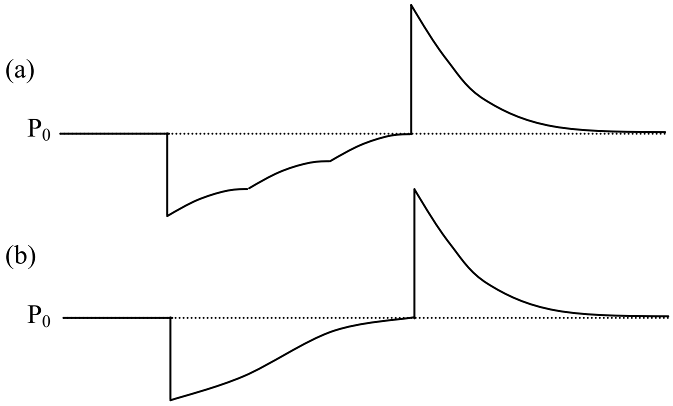


Figure 7.18. Example of (a) actual and (b) load model transient response.

7.3.1 Same Power, Different Capacitance

Each load is approximately 90W with an equivalent capacitance of 800, 1500, and 2500uF. The model parameters and determined characteristics for the individual and composite loads are shown in Table 7.4. Characteristics λ and *k* do not apply for the individual loads but have been included to show their composite distribution characteristics.

Table 7.4. Load Model Parameters and Transient Characteristics for: Small Transformer Tests – Same Power, Different Capacitance.

P (W)	Sag (Vpu)	C_{eq} (uF)	R (ohm)	L (mH)	$V_{capSSpf}$ (V)	V_{capSSf} (V)	μ (sec)	τ_f (sec)	τ_{fscale}	λ (sec)	k	τ_{pf} (sec)	$\tau_{pfscale}$
93	0.7	800	2	9	155	104	0.043	0.012	3.815	0.058	2.702	0.004	1.228
87	0.7	1500	2	9	154	104	0.083	0.027	4.615	0.118	2.467	0.010	1.698
89	0.7	2500	2	9	154	103	0.135	0.050	5.077	0.199	2.310	0.018	1.835
269	0.7	4800	1.2	5	149	98	0.072	0.042	3.883	0.123	1.855	0.018	1.676

The actual 90W load responses in Figures 7.19, 7.20, and 7.21 are due to 800, 1500, and 2500uF equivalent load capacitance, respectively when subjected to a ten cycle 30% voltage sag. The low system impedance along with the low storage factor leads to the fast post-fault time constant seen in Figure 7.19. The post-fault recovery overshoots the steady state capacitor voltage, and therefore, the capacitor discharges for an additional cycle.

The fault and post-fault time constants increase as the load capacitance increases. Time constant τ_f has a scale factor of approximately 4, and τ_{pf} has a scale factor of approximately 1.5 due to the low fault voltage.

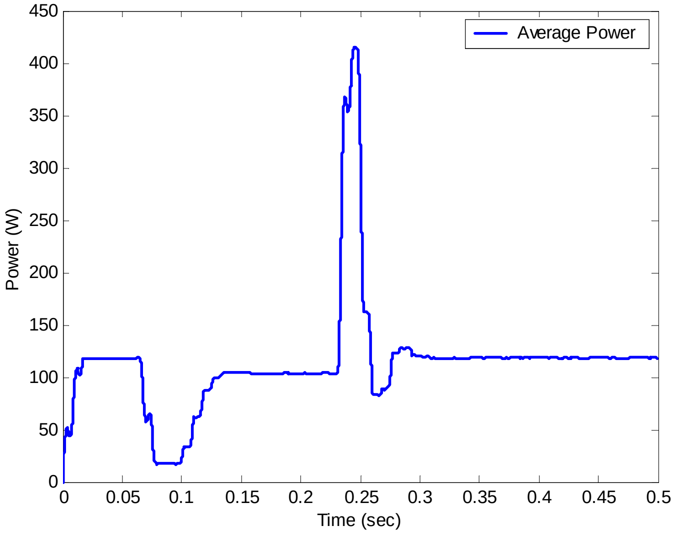


Figure 7.19. 93W actual individual power electronic load response.

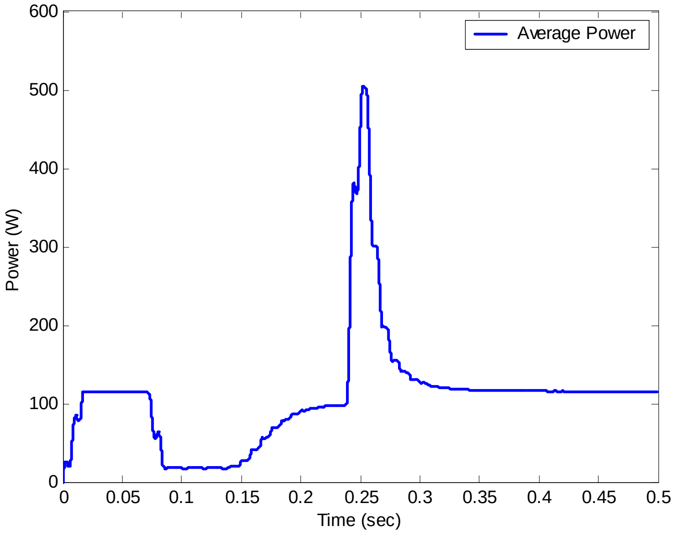


Figure 7.20. 87W actual individual power electronic load response.

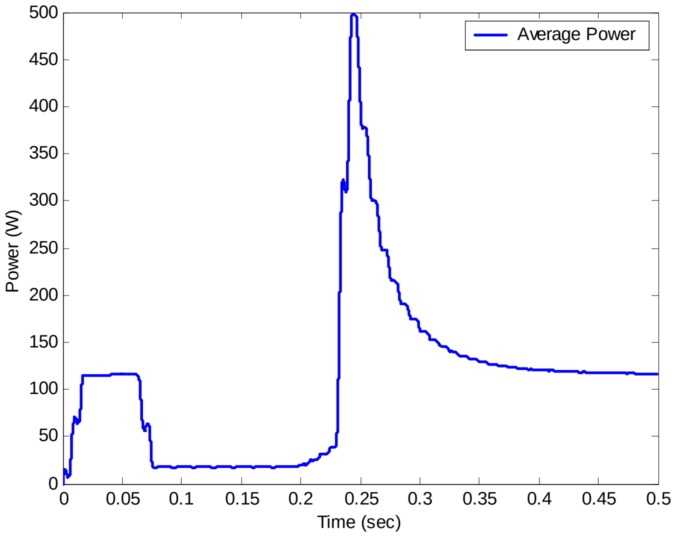


Figure 7.21. 89W actual individual power electronic load response.

The composite load response in Figure 7.22 is the sum of the previous three individual load responses. One can see the individual loads reconnect in the fault in Figure 7.22.

The system impedance decreases for the parallel composite load while the composite capacitance increases. The decrease in system impedance causes the steady state composite capacitor voltage to remain above the peak fault voltage even though the load has increased. Therefore, the composite load fault response has a ride-through, and the distribution shape is greater than exponential. Time constant λ is approximately $\mu + \tau_f$. The power electronic model response in Figure 7.23 is generated using the transient characteristics for the composite load.

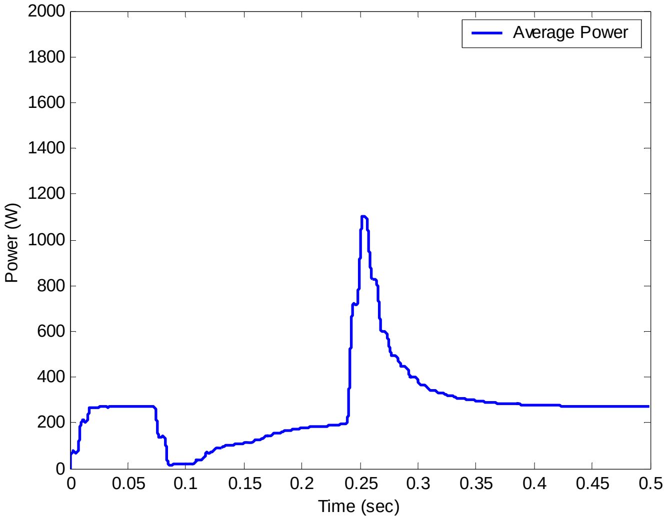


Figure 7.22. 269W actual composite power electronic load response.

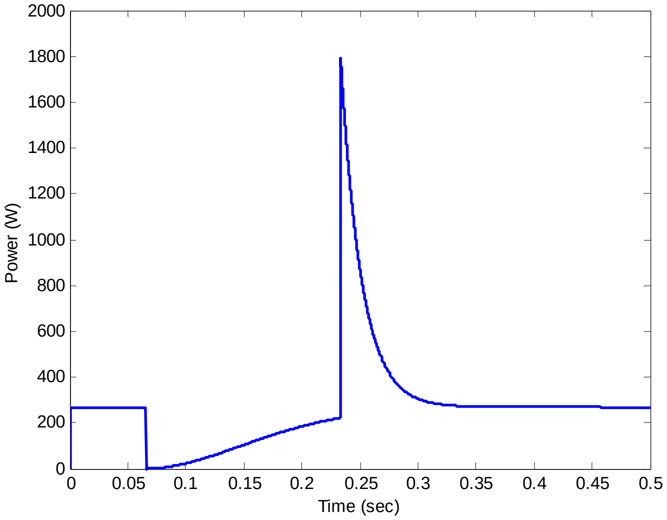


Figure 7.23. Power electronic load model response of Figure 7.22.

7.3.2 Same Capacitance, Different Power

The individual loads with the same capacitance and different power have similar responses to the previous five figures; however, the large load dominates the impact on the composite load response. The individual load powers are 42, 57, and 87W. Each load has an equivalent capacitance of 1500uF and experiences a ten cycle 20% voltage sag. The individual and composite load model parameters and determined transient characteristics are given in Table 7.5. Characteristics λ and *k* do not apply for the individual loads but have been included to show their composite distribution characteristics.

Table 7.5. Load Model Parameters and Transient Characteristics for: Small Transformer Tests – Same Capacitance, Different Power.

P (W)	Sag (Vpu)	C_{eq} (uF)	R (ohm)	L (mH)	$V_{capSSpf}$ (V)	V_{capSSf} (V)	μ (sec)	τ_f (sec)	τ_{fscale}	λ (sec)	k	τ_{pf} (sec)	$\tau_{pfscale}$
42	0.8	1500	2	9	159	125	0.122	0.049	8.329	0.185	2.211	0.015	2.474
57	0.8	1500	2	9	157	123	0.082	0.043	7.217	0.135	1.944	0.014	2.279
87	0.8	1500	2	9	154	121	0.046	0.032	5.331	0.083	1.717	0.012	2.062
192	0.8	4500	1.2	5	152	118	0.055	0.054	5.368	0.118	1.504	0.021	2.103

Figures 7.24, 7.25, and 7.26 show the responses for the 42, 57, and 87W loads, respectively. Due to the large storage factors, τ_{fscale} is greatly increased. Time constant τ_{pf} has a scale factor of approximately 2.2.

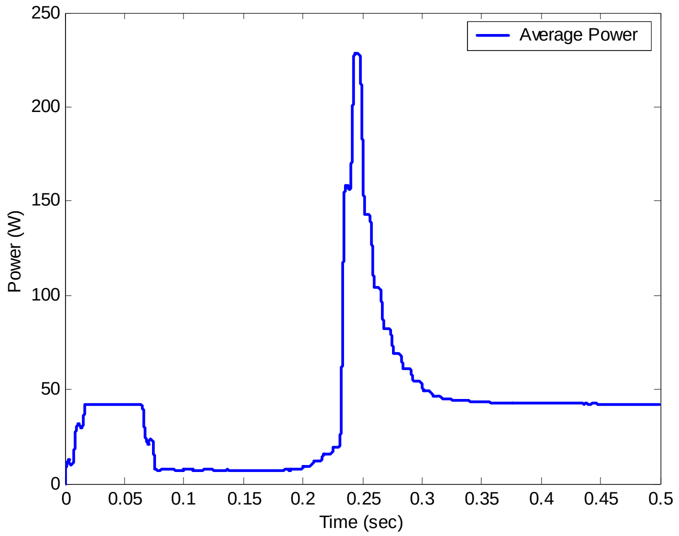


Figure 7.24. 42W actual individual power electronic load response.

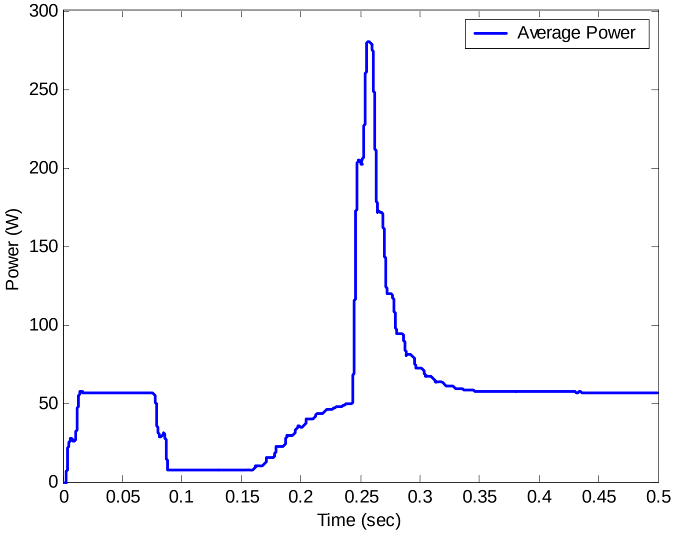


Figure 7.25. 57W actual individual power electronic load response.

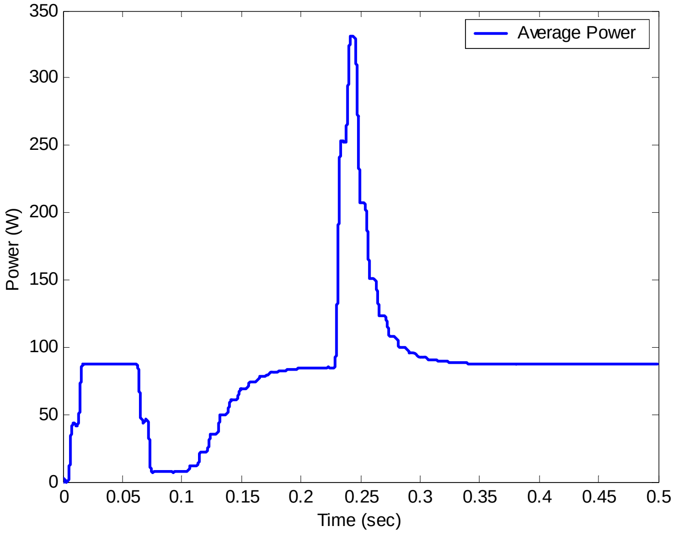


Figure 7.26. 87W actual individual power electronic load response.

The composite load is the sum of the individual load responses as seen in Figure 7.27. The load capacitance triples while the impedance decreases by approximately a factor of two. Therefore, time constant τ_{pf} only slightly increases. The fault distribution shape is greater than one and λ is approximately $\mu + \tau_f$. The transient power electronic load model characteristics are used to attain the response in Figure 7.28.

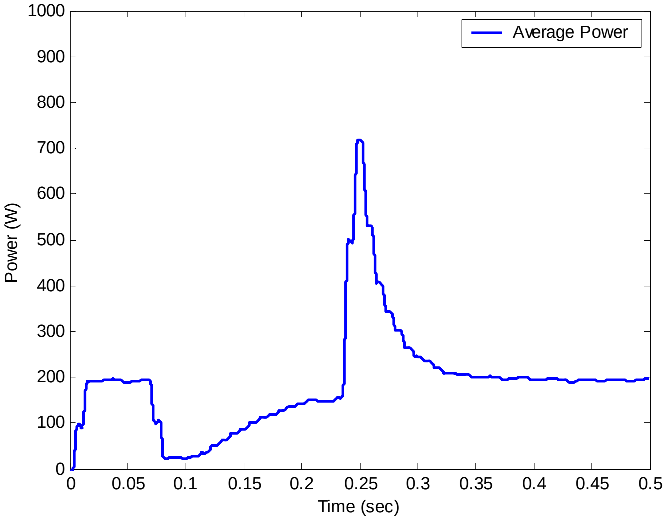


Figure 7.27. 192W actual composite power electronic load response.

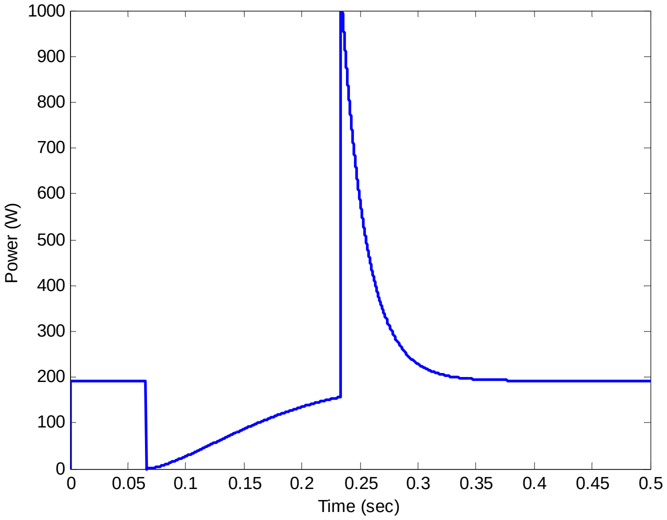


Figure 7.28. Power electronic load model response of Figure 7.27.

7.4 SUMMARY

The analytical dynamic equations from Chapter 5 are used to solve the composite load transient characteristics when the actual load model parameters are known. The response of the derived model compares favorably to the actual composite load. The results therefore validate the transient power electronic load model.

From the actual load response, the following observations are made during the fault which corresponds to previous theoretical predictions:

- The individual load exponentially reconnects to the system in the fault.
- The composite load recovers as a Weibull CDF.
- The composite load distribution shape k is greater than one when the steady state capacitor voltage is above the peak fault voltage.
- The fault response shape is one (exponential) when the steady state capacitor voltage is less than or equal to the peak fault voltage.
- Weibull time constant λ is approximately $\mu + \tau_f$.
- Ride-through time μ is dependent on the storage factor and voltage sag.
- Exponential time constant τ_f is approximately $3\left|Z_{line}\right| \cdot C$.

The following observations are made for the post-fault response that agrees with previous predictions:

- The post-fault response is an Exponential PDF.
- The inrush is dependent on the energy discharged by the capacitor during the fault and the post-fault time constant.
- The post-fault time constant τ_{pf} can be closely estimated using $1.5\left|Z_{line}\right| \cdot C$.
- Time constant τ_{pf} is approximately half τ_f.

Summarizing, the transient power electronic load model accurately represents the behavior of composite loads when subjected to voltage sags. If the composite load model parameters are known, the transient model characteristics can be solved analytically.

Chapter 8 – Utility Composite Power Electronic Load Response

The actual utility feeder data first examined in Chapter 3 is reexamined here to determine the utility composite power electronic load model parameters and transient characteristics. The composite utility power electronic load response is evident in the current waveform (solid line) shown in Figure 8.1. The power electronic load increases in the fault and is followed by an inrush for several cycles after the fault is cleared. Due to the varied composition of the total utility power electronic load, the composite load response is unique depending on the event. In this chapter, I derive the utility power electronic load parameters and characteristics using the dynamic equations and observing the actual load response.

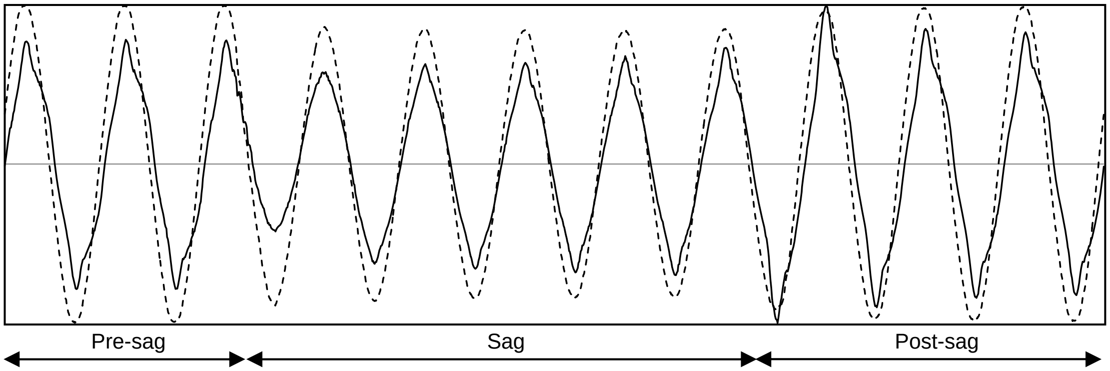


Figure 8.1. Utility load response due to a voltage sag (Dashed line is voltage, solid line is current).

8.1 COMPOSITE LOAD MODEL PARAMETERS

Unlike the power electronic load in Chapter 7, the system composite load model parameters are unknown. The composite load power is best estimated using the decomposition procedure explained in Chapter 3, and the composite load capacitance is estimated assuming the average load has a 5% capacitor voltage ripple. Operating at peak voltage (10.5kV), the approximate storage factor rating is 0.77nF/W. Total load capacitance therefore depends on the total load power. The best estimate for composite load system impedance is determined by curve fitting the load model response to the actual power electronic load response.

The appropriate steady state current waveform is attained with low line impedance (i.e., ≈ 0.5ohm and 10mH) which is due to the impedance from the source to the network bus. This impedance is used to simulate the waveform seen in Figure 8.2. The actual composite power electronic load response during a voltage sag, however, is dependent on a larger value of line impedance (i.e., ≈ 15ohm and 75mH) due to the individual load impedances referred to the to the utility voltage by the transformer turns ratio.

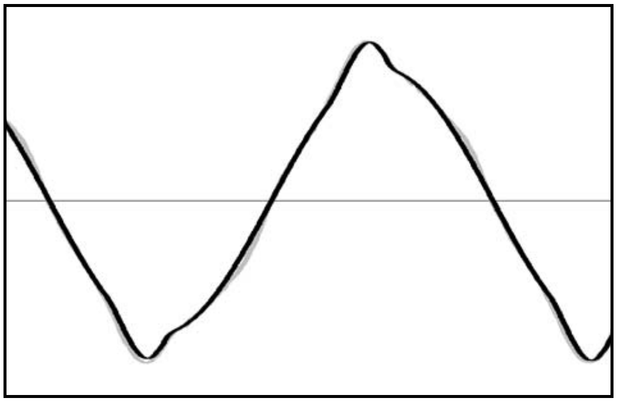


Figure 8.2. Actual (gray line) and simulated (black line) load current.

If the composite power electronic load is located near the substation, the source impedance is low. A schematic of this load distribution is shown in Figure 8.3. The source impedance is effectively 2Z to the composite load at the point of common coupling. The individual loads (represented by load impedance Z followed by load capacitor C) at the point of common coupling are effectively in parallel and therefore have less effective impedance as shown in Chapter 7. In Figure 8.3, the parallel load impedance is effectively 0.2Z. Overall, the source impedance and parallel load impedance are low, thus resulting in low (2.2Z) system impedance (i.e., system impedance is defined as source plus load impedance).

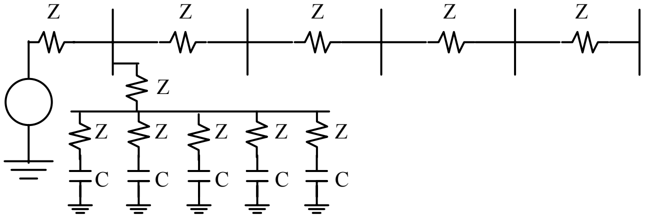


Figure 8.3. Schematic of power electronic loads distributed near source.

The resulting time constants and responses are fast. A response of this sort is shown in Figure 8.4. The composite load immediately comes online in the fault after the ride-through with a normal distribution shape and a time constant slightly longer than the ride-through time. The post-fault inrush over-charges the capacitor in less than one cycle causing the load to ride through the following cycle. This response can occur, however, the load is typically more distributed over the line.

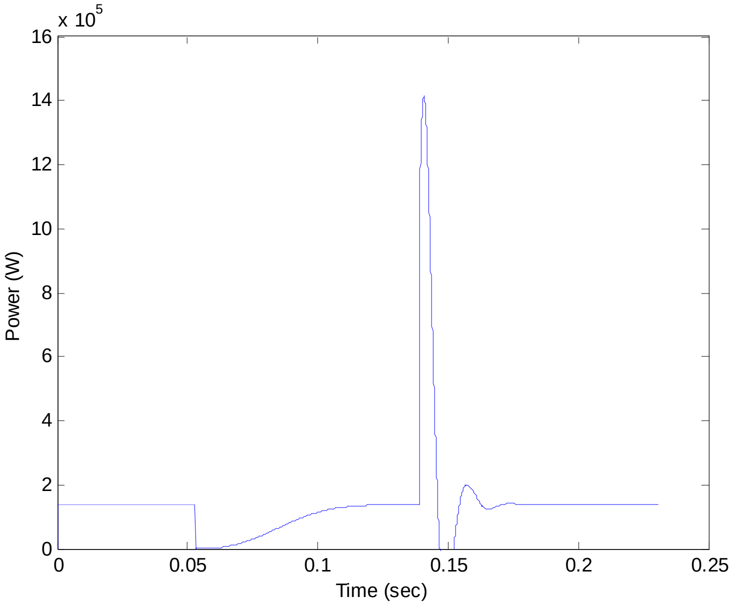


Figure 8.4. Response of utility power electronic load located near source.

The system impedance increases when the utility power electronic load is distributed across the distribution system. A schematic of the distributed load can be seen in Figure 8.5. The additional impedance is partly due to the weighted average source impedance to the distributed load (4Z). Fewer loads are also in parallel at the points of common coupling so the parallel load impedance at each point of common coupling increases (1Z). The weighted average system impedance to the distributed load is effectively 5Z.

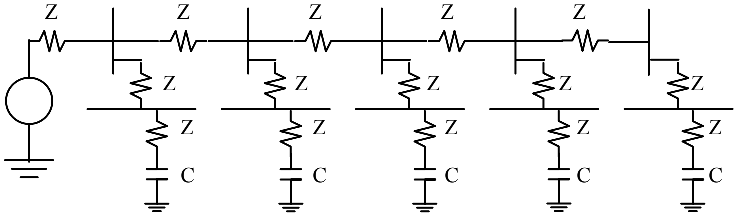


Figure 8.5. Schematic of power electronic loads distributed over system.

Greater system impedance decreases the steady state capacitor voltage, increases the composite load time constant, and spreads the response over the fault as seen in Figure 8.6. The fault response shape is close to exponential and the load comes online faster at the onset of the fault. The post-fault time constant is primarily affected by the increase in line impedance. The capacitor restores over several cycles which decreases the initial inrush.

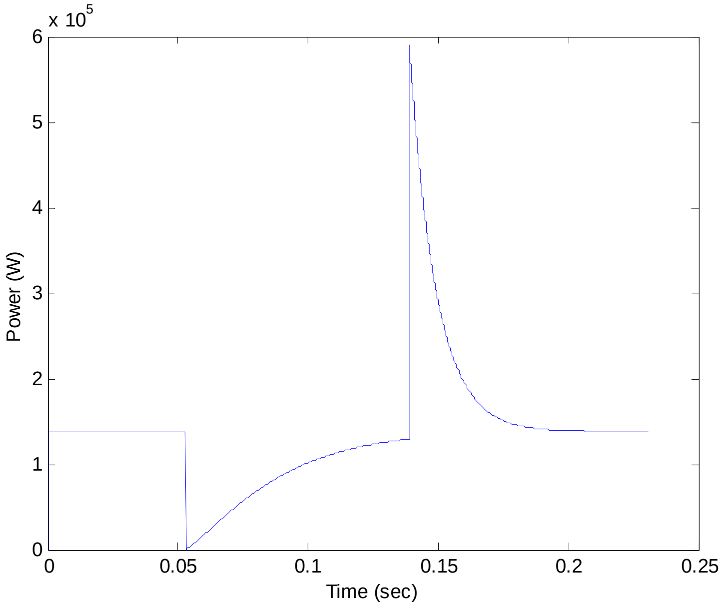


Figure 8.6. Response of utility power electronic load distributed across system.

If the entire power electronic load is located in the center of the line, the effective system impedance would be 4.2Z. If the entire power electronic load is located at the end of the distribution line, the effective impedance would be 6.2Z. If 80% of the total load is located near the source and 20% is located at the end of the line, the effective impedance is found by the weighted average and would be 3.2Z. If the load increases distributed evenly over the entire distribution system, the parallel load impedance would decrease at each point of common coupling. The system impedance would decrease to 4Z.

The composite load power and capacitance can be estimated, however, the composite load impedance is dependent on the load and the load distribution. The effective impedance of the composite load is determined in the following section using the actual load response.

8.2 SIX SELECTED EVENTS

The load model characteristics for six events occurring on the Brodie Lane substation are presented here. The first event occurred in the morning in the month of November on phase C. The second event occurred in the evening in the month of December on phase A. The third event occurred in March in the evening on phase C. The last three events occurred simultaneously on the three phases in the month of December. The last three events occur in the afternoon two years prior to the first three events.

The system impedance, capacitance, and power are different in each case and therefore, the power electronic responses are different. I used the utility model assumptions and adjusted the system impedance and capacitance to attain a good fit between the simulated power electronic load response and actual field data. The power electronic load characteristics are also found by observing the actual AC current, RMS current, and average power response data.

The power electronic load transient characteristics for the six events are given in Table 8.1. The fault time constants are approximately twice as long as the post-fault time constants. The average fault time constant is 0.04 seconds while the average post-fault time constant is 0.015 seconds.

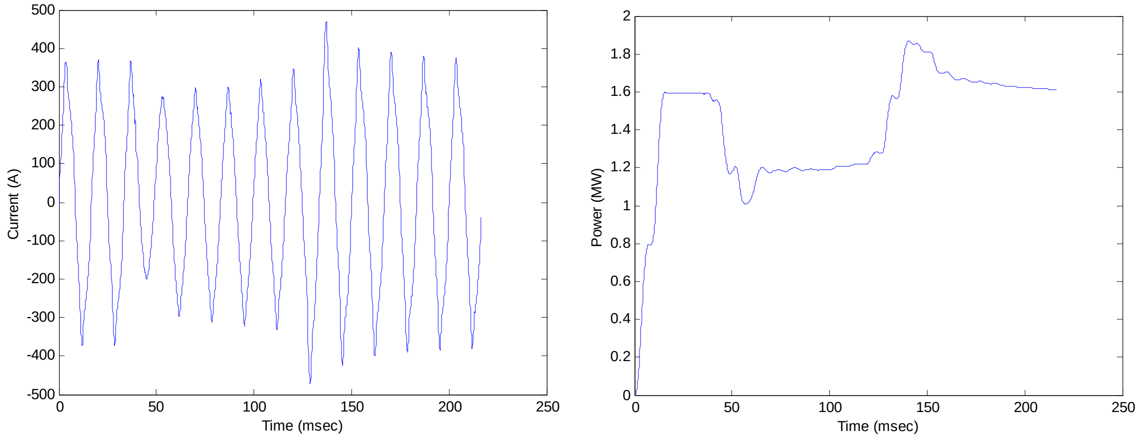
Table 8.1. Utility Event Parameters and Characteristics.

Event	PE Power (MW)	Sag (pu)	λ	k	τ_{pf}
Nov. 23, 2004 9:47:05 Phase C	0.138	0.84	0.04	1.1	0.017
Dec. 29, 2004 1:55:36 Phase A	0.171	0.79	0.02	1.8	0.006
Mar. 25, 2005 22:35:57 Phase C	0.174	0.88	0.05	1.0	0.02
Dec. 30, 2002 16:24:41 Phase A	0.158	0.77	0.05	1.2	0.02
Dec. 30, 2002 16:24:41 Phase B	0.159	0.76	0.04	1.1	0.012
Dec. 30, 2002 16:24:41 Phase C	0.146	0.77	0.04	1.1	0.012

8.2.1 November 23, 2004 Phase C

The power electronic load time constants and fault shape are best determined directly from the actual AC current, RMS current, or average power response data. The actual AC current response for the November event can be seen in Figure 8.7a. The power electronic load comes online at the onset of the fault and increases until the fault clears. The fault shape is near exponential with a time constant of approximately two to three cycles. The load is most likely evenly distributed over the feeder. The post-fault current response takes approximately 3 cycles to reach a steady state. Assuming the exponential decay is near zero after 3 time constants, the visual post-fault time constant would be 1 cycle (0.0167 seconds). Figure 8.7b shows the total average power response for the actual event. Due to a low pass filtering effect when averaging the waveform, sudden transitions appear more gradual. The increase in power during the fault can be seen followed by the post-fault inrush after the fault is cleared.

The power electronic load response using the determined time constants and shape from Table 8.1 is shown in Figure 8.8. The energy dissipated from the capacitor during the fault is restored during the inrush after the fault.



(a) (b)

Figure 8.7. Actual (a) total load current and (b) active power response for Nov 23, 2004 event.

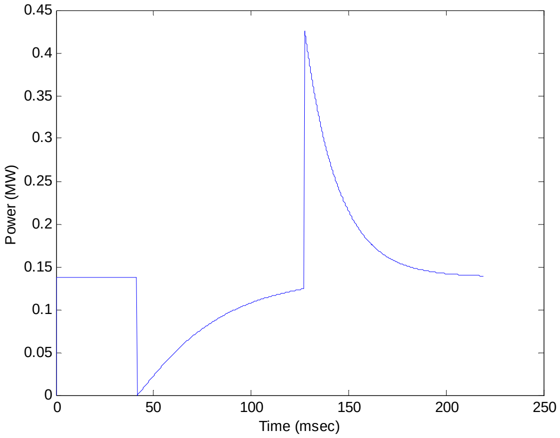
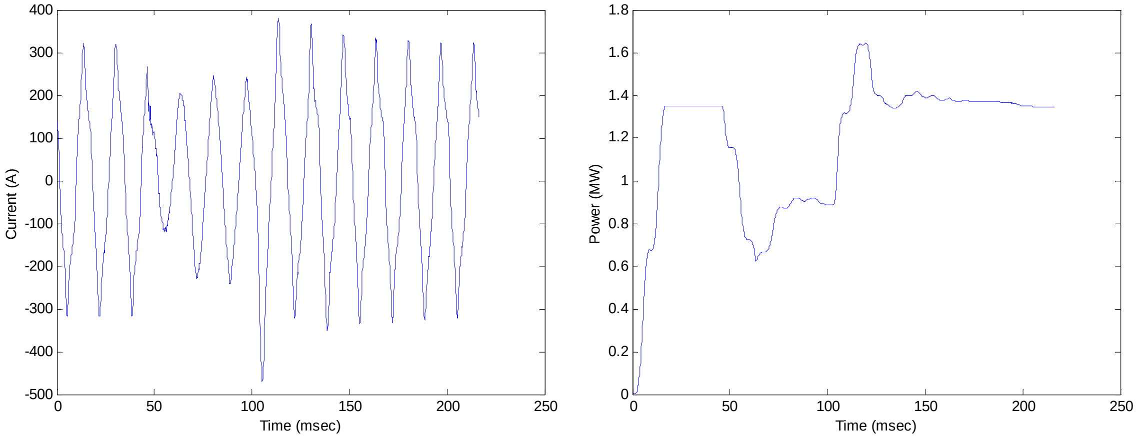


Figure 8.8. Power electronic load model response for November 23, 2004 event.

8.2.2 December 29, 2004 Phase A

The actual load current response for the December 29, 2004 event can be seen in Figure 8.9a followed by the total average power response in Figure 8.9b. The load is mostly disconnected during the first cycle in the fault and then quickly reaches a steady state in the following cycles. The post-fault response is also fast. In the actual current waveform, the power electronic load restores for one cycle in the post-fault and then skips a half cycle. This is indicative of the capacitor overcharging and riding through a half cycle. These responses suggest low capacitance and system impedance which can be caused by the composite load located near the substation. The fault response shape is exponential with an approximate one cycle time constant. The determined power electronic fault response is shown in Figure 8.10 using the parameters from Table 8.1.



(a) (b)

Figure 8.9. Actual (a) total load current and (b) active power response for Dec 29, 2004 event.

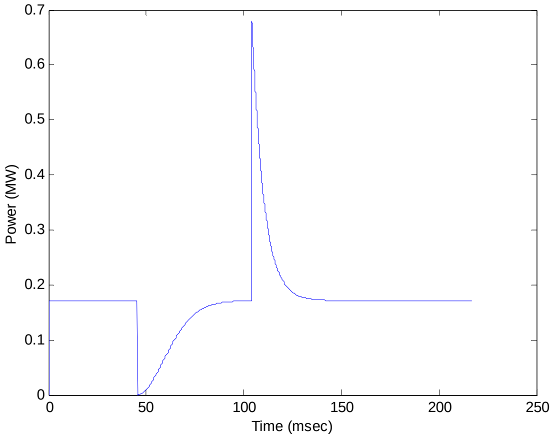
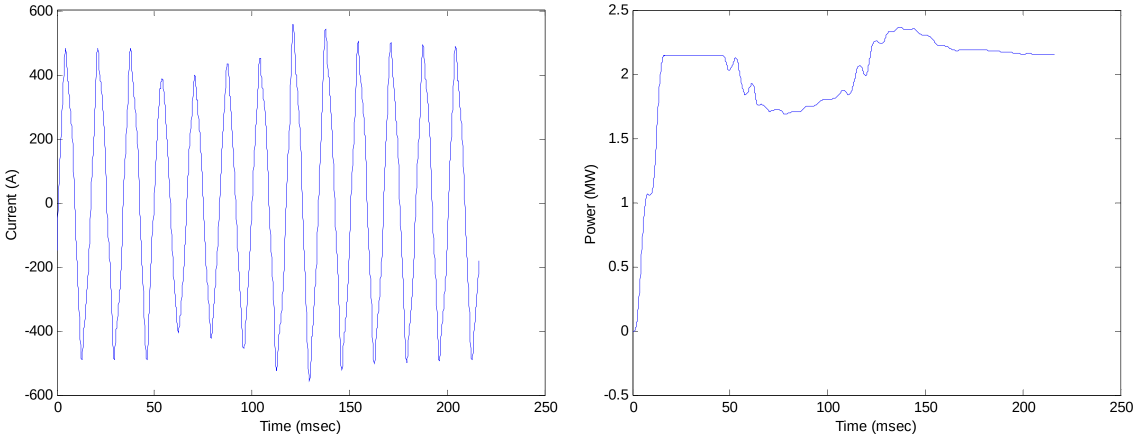


Figure 8.10. Power electronic load model response for December 29, 2004 event.

8.2.3 March 25, 2005 Phase C

The actual fault response data for the March event are shown in Figure 8.11. The composite load slowly increases during the onset of the fault. Because the fault voltage is 0.88pu, a portion of the load is online at the onset of the fault. The slow increase in load is due to a long time constant. The power electronic load still has not reached a steady state when the fault clears. Therefore, the fault time constant is several cycles long. The post-fault response is also longer than the previous two cases. The composite power electronic load is most likely located near the end of the feeder which results in greater system impedance. The simulated power electronic load response is shown in Figure 8.12.



(a) (b)

Figure 8.11. Actual (a) total load current and (b) active power response for March 25, 2005 event.

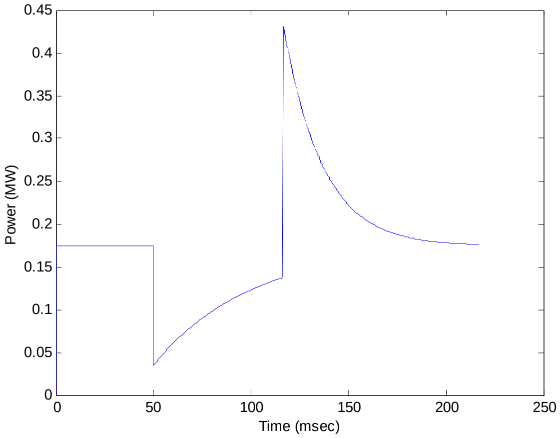
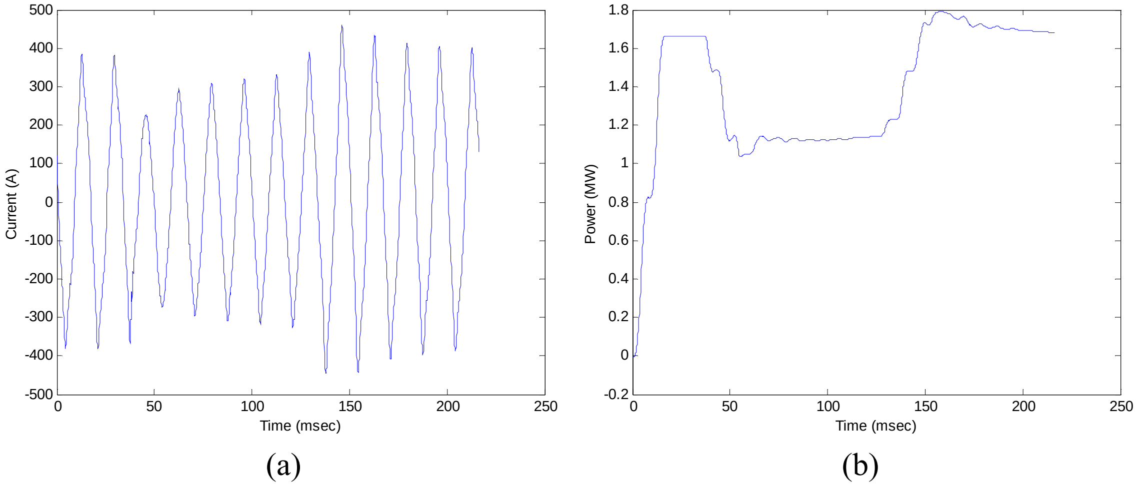


Figure 8.12. Power electronic load model response for March 25, 2005 event.

8.2.4 December 30, 2002 Phase A

The actual response data for the December 2002 Phase A event are shown in Figure 8.13. The power electronic load increases over the complete fault; however, the load has not reached steady state by the end of the fault. The post-fault response gradually reaches a steady state over more than three cycles. The long post-fault time constants suggest the composite load experiences high impedance and is most likely located near the end of the feeder. The simulated power electronic load response can be seen in Figure 8.14.



(a) (b)

Figure 8.13. Actual (a) total load current and (b) active power response for Dec 30, 2002 Phase A event.

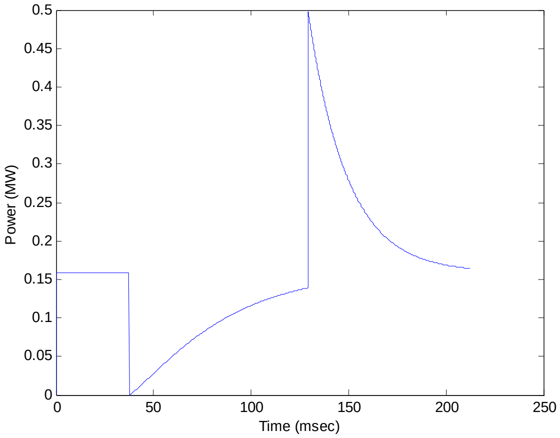
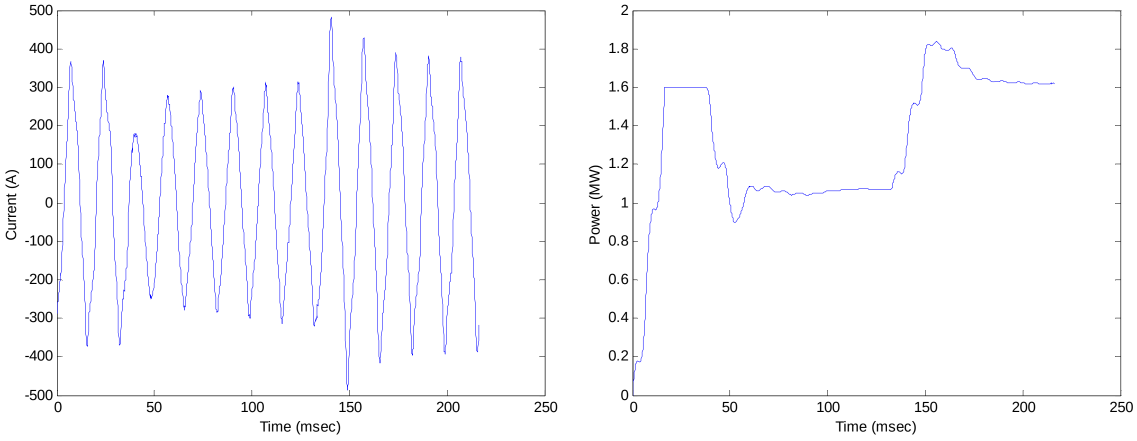


Figure 8.14. Power electronic load model response for Dec 30, 2002 Phase A event.

8.2.5 December 30, 2002 Phase B

The actual response data for the December 2002 Phase B event are shown in Figure 8.15. The load quickly connects to the system at the onset of the fault and reaches near steady state by fault clearing. The post-fault response is also faster than that on Phase A. Therefore, the composite load is most likely distributed over the feeder. The simulated response is shown in Figure 8.16 using the load characteristics from Table 8.1.



(a) (b)

Figure 8.15. Actual (a) total load current and (b) active power response for Dec 30, 2002 Phase B event.

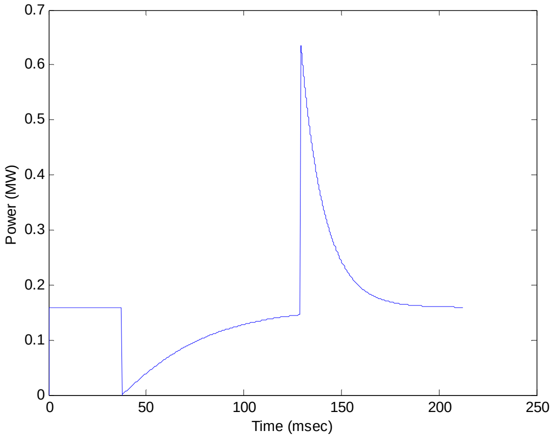
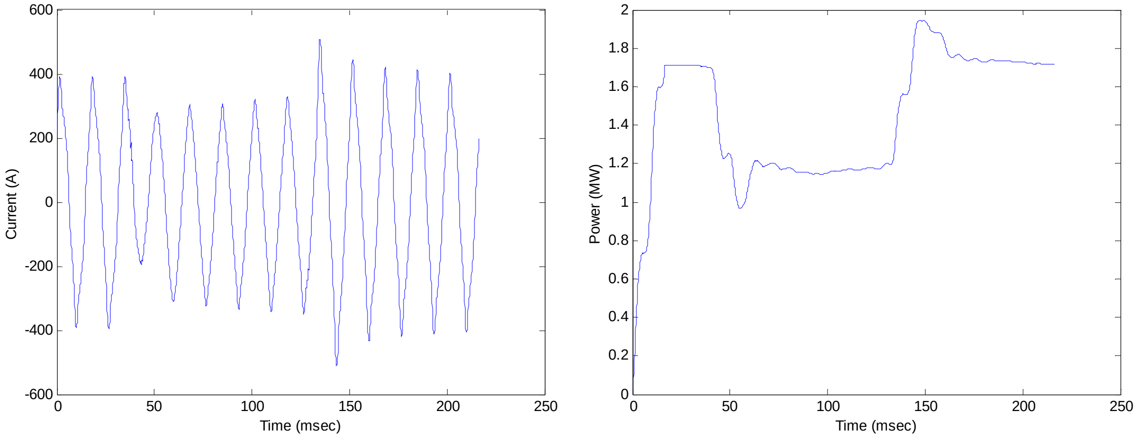


Figure 8.16. Power electronic load model response for Dec 30, 2002 Phase B event.

8.2.6 December 30, 2002 Phase C

The actual response data for the December 2002 Phase C event are shown in Figure 8.17. The load response is similar to that on Phase B. The simulated response using the load characteristics from Table 8.1 is shown in Figure 8.18.



(a) (b)

Figure 8.17. Actual (a) total load current and (b) active power response for Dec 30, 2002 Phase C event.

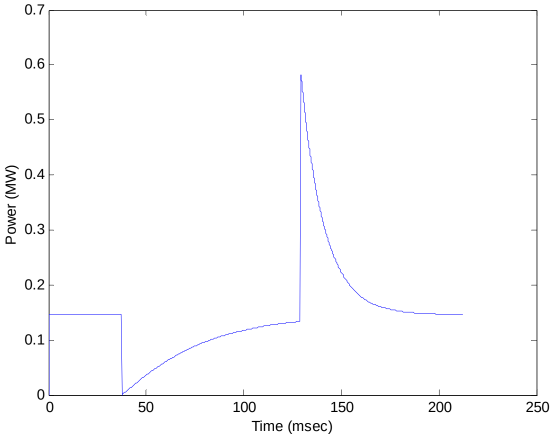


Figure 8.18. Power electronic load model response for Dec 30, 2002 Phase C event.

8.3 SUMMARY

Observing actual utility fault response data, the appropriate Weibull CDF fault time constant λ, fault shape k, and Exponential PDF post-fault time constant τ_{pf} can be estimated. The shape and time constants of the utility power electronic load are dependent on the size of the load, effective impedance, storage factor, and voltage sag. The average utility load response is best described with

- $\lambda = 0.04$sec
- $k = 1.1$, and
- $\tau_{pf} = 0.015$.

The utility events studied in this chapter represent moderate voltage sags and percentage of power electronic load for a specific residential feeder. The response, however, can be different for other feeders with different impedance (i.e., rural feeders), more power electronic load, or if the voltage sag had been different. Observing the actual response for other feeders would give the best characteristics for those composite loads.

For the following three scenarios, the load model characteristics are estimated from the results provided by the simulated load in Figures 6.7, 6.13, and 6.14 of Chapter 6.

- If the voltage sag increases, the fault response shape increases because the load ride-through time μ increases. However, the fault time constant λ only slightly increases because τ_f decreases slightly due to a lower τ_{fscale} (i.e., $\lambda \approx \mu + \tau_f$). The post-fault time constant decreases slightly as $\tau_{pfscale}$ decreases.
- If the power electronic load increases on the same feeder, the capacitance will increase, however, the effective impedance and scale factors will decrease. Time constant τ_{pf} only slightly decreases. The fault time constant λ only slightly decreases because the ride-through time μ decreases and τ_f slightly increases.

(i.e., $\lambda \approx \mu + \tau_f$). The fault response shape becomes more exponential due to the lower pre-fault steady state capacitor voltage.

- If both the power electronic load and voltage sag increase, the fault time constant and shape remain approximately the same while the post-fault time constant decreases slightly.

Chapter 9 – Impact of Power Electronic Loads on Power System Transient Response and Stability

A generalized state-space averaging method was developed in [25] to model power electronic loads in AC distribution systems and determine small signal stability issues. The study established that the constant power drawn by the power electronic load has a negative impedance characteristic and can lead to negative impedance instability. To ensure small signal stability, these loads must be less than the fraction of other loads on the power system.

The large signal transient model developed in this dissertation represents the average system power drawn by the power electronic loads neglecting their associated harmonics. The transient response of these loads is unique compared to traditional linear loads. This chapter examines the impact of power electronic loads on power system transient response and stability using the developed model.

9.1 TRANSIENT ENERGY ANALYSIS

A special case of Lyaponov's direct method for transient energy analysis, the energy method, uses transient energy functions (TEF) for all system components to assess power system transient stability. The system, disturbed by a fault, causes the synchronous machines to accelerate. During the fault, the generators gain potential and kinetic energy while moving away from the stable equilibrium point (SEP). When the fault clears, the system must be able to absorb the gained energy before moving past the potential energy boundary surface (PEBS) to bring the system back to a SEP [2].

Picture the power system as a bowl and the SEP is the resting point of the ball at the bottom as in Figure 9.1. When a disturbance occurs, energy is injected into the ball and the ball begins to move away from the SEP. The ball will travel up the inside of the bowl along a specific path depending on the initial kinetic energy. If the gained energy in the ball is greater than the rim's PEBS along the trajectory, the ball will enter a region of instability.

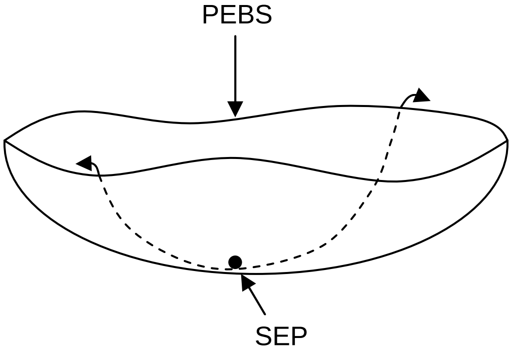


Figure 9.1. Ball analogy for system transient stability.

Elaborate systems including load models such as power electronics require new functions defining transient energy. In the TEF, the load is typically represented as constant impedance and included in the admittance matrix. New models have been developed, however, to represent the load as constant current or MVA. The transient energy of theses loads are then included to determine the total system energy.

9.1.1 Complex System

A positive power imbalance in a synchronous machine will cause the rotor to accelerate. Kinetic and potential energy build up in the generator and the system moves away from the SEP. The clearing energy is the total system energy injected into the system at fault clearing and is described as

$$W_{cl} = W_{KE} - W_{PE} = \frac{1}{2}\sum_{i=1}^{n} J_i \omega_i^2 - \int_{\theta_i^{SEP}}^{\theta_i^{cl}} \left(P_{mi} - P_{ei}\right) d\theta \qquad (9\text{-}1)$$

which expands to

$$W_{cl} = \frac{1}{2}\sum_{i=1}^{n} J_i \omega_i^2 - \sum_{i=1}^{n} P_{mi}\left(\theta_i^{cl} - \theta_i^{SEP}\right) - \sum_{i=1}^{n-1}\sum_{j=i+1}^{n}\left[E_i E_j B_{ij}\left(\cos\theta_{ij}^{cl} - \cos\theta_{ij}^{SEP}\right) - \int_{\theta_i^{SEP}+\theta_j^{SEP}}^{\theta_i^{cl}+\theta_j^{cl}} E_i E_j G_{ij} \cos\theta_{ij} d\left(\theta_i + \theta_j\right)\right] \quad (9\text{-}2)$$

The first term is the rotor kinetic energy of all generators in the center of inertia reference frame. The second term is the rotor potential energy of all the generators relative to the center of inertia. The third term is the stored magnetic energy of all branches, and the last term is the dissipated energy of all branches. All variables are explained in [2].

The potential energy absorbing capability of the system at the PEBS must be greater than the accumulated energy at fault clearing in order for the system to remain stable. The critical energy is the system's energy absorbing capability at the unstable equilibrium point (UEP) on the PEBS and is described as

$$W_{cr} = -\sum_{i=1}^{n} P_{mi}\left(\theta_i^{UEP} - \theta_i^{SEP}\right) - \sum_{i=1}^{n-1}\sum_{j=i+1}^{n}\left[E_i E_j B_{ij}\left(\cos\theta_{ij}^{UEP} - \cos\theta_{ij}^{SEP}\right) - \int_{\theta_i^{SEP}+\theta_j^{SEP}}^{\theta_i^{UEP}+\theta_j^{UEP}} E_i E_j G_{ij} \cos\theta_{ij} d\left(\theta_i + \theta_j\right)\right] \quad (9\text{-}3)$$

The difficulty of this analysis is the determination of the UEP. To maintain stability,

$$W_{cr} - W_{cl} > 0\,. \quad (9\text{-}4)$$

9.1.2 Classical One Generator-Infinite Bus Example

For a well defined system involving one generator transmitting power to an infinite bus and ignoring the energy dissipated from all branches, the total clearing energy simplifies to

$$W_{cl} = \frac{1}{2} J\omega_r^2 - P_m\left(\theta_{cl} - \theta_{SEP}\right) - \frac{E'V_\infty}{X_T}\left(\cos\theta_{cl} - \cos\theta_{SEP}\right) \quad (9\text{-}5)$$

where θ_{SEP} is the initial rotor angle, V_∞ is the infinite bus voltage, E' is the generator transient voltage, X_T is the impedance between the infinite bus and the generator including the generator transient reactance, θ is the angle at which E_a' leads V_∞, J is the moment of inertia of the generator, and P_m is the mechanical power input. The clearing angle θ_{cl} and rotor speed ω_r are found by running a simulation until the fault is cleared. The critical energy simplifies to

$$W_{cr} = -P_m\left(\theta_{UEP} - \theta_{SEP}\right) - \frac{E'V_\infty}{X_T}\left(\cos\theta_{UEP} - \cos\theta_{SEP}\right) \tag{9-6}$$

where θ_{UEP} is the unstable rotor angle. Using (9-4), stability is maintained when

$$A_1 - \frac{1}{2}J\omega_r^2 > 0 \tag{9-7}$$

where A_1 is equal to the area of the shaded region in Figure 9.2. For the well defined system, the power-angle curve in Figure 9.2 can be used to determine system stability. This approach is similar to the equal area criterion.

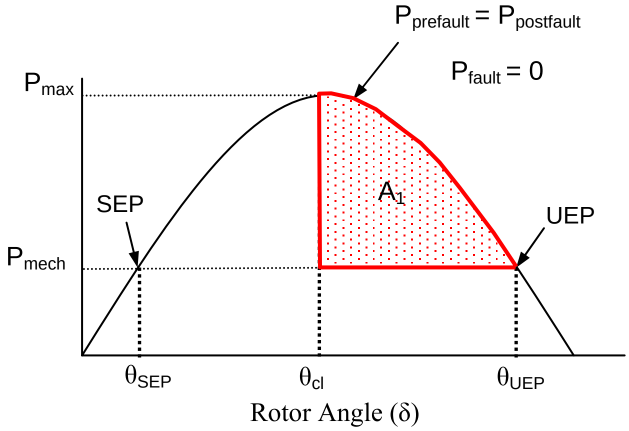


Figure 9.2. Transient energy analysis using power-angle curve.

9.2 EQUAL AREA CRITERION

The Equal Area Criterion (EAC) is a simplex form of the TEF analysis for well defined systems. The EAC graphically analyzes the bounds for stable operation with the power-angle curve shown in Figure 9.3. This method of analysis is based on the swing equation; however, the method is not intended for multi-machine stability and is only appropriate when the problem is well defined [2].

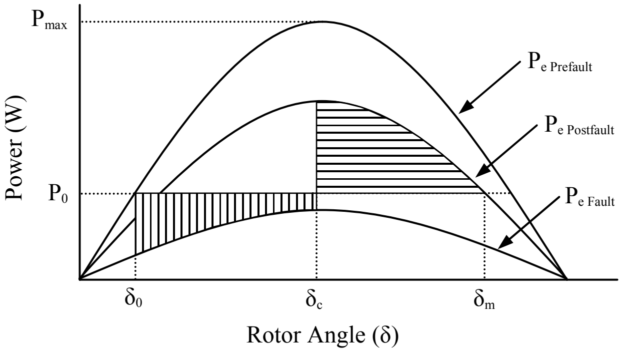


Figure 9.3. Equal area criterion using power-angle curve.

The electrical power output of the generator can be described as

$$P_e = \frac{\left|E_a{}'\right| \cdot \left|V_L\right|}{X_T} \sin(\delta). \tag{9-8}$$

where V_L is the reference bus voltage, $E_a{}'$ is the generator transient voltage, X_T is the impedance between the reference bus and the generator including the generator transient reactance, and δ is the angle at which $E_a{}'$ leads V_L.

Before the fault occurs, the system is assumed to be in a state of equilibrium where the electrical power output P_e is equal to the mechanical power input P_m which is the initial operating condition P_0 at angle δ_0. When the fault occurs, the electrical power output curve decreases due to the change in impedance or reference bus voltage. Meanwhile, the mechanical input remains constant assuming no governor control. The kinetic energy accumulated in the synchronous machine is the difference between the mechanical power input and the electrical output as the generator rotor angle increases. The kinetic energy is indicated by the vertically shaded region in Figure 9.3. When the fault clears, the accumulated energy must be absorbed by the system before the unstable equilibrium point δ_m to return to a stable mode of operation. The critical energy absorbed by the system is the difference between the post-fault electrical power output and the mechanical power input as the rotor angle continues to increase. The absorbed critical energy is shown by the horizontally shaded region in Figure 9.3. If the energy absorbed by the system (horizontally shaded region) does not at least match the energy accumulated by the synchronous machine during the fault (vertically shaded region), the machine will continue to accelerate out of equilibrium. Equating these two areas,

$$\int_{\delta_o}^{\delta_c} (P_m - P_e) d\delta = \int_{\delta_c}^{\delta_m} (P_e - P_m) d\delta , \tag{9-9}$$

allows one to solve the critical clearing angle δ_c which is the furthest the rotor angle can swing before going unstable.

9.3 THE UNIVERSITY OF TEXAS AT AUSTIN CAMPUS POWER SYSTEM

The University of Texas at Austin has a unique power system in which the university load is met by on-campus generation. The campus power system is connected to the city of Austin and the rest of ERCOT (Electric Reliability Council of Texas); however, this is only for frequency and voltage support. Data has been collected for the UT system through cooperation of personnel in the UT Power Plant to provide accurate model parameters. The UT generator and exciter data are included in Appendix F.

Figure 9.4 shows the one-line diagram for the UT power system. The generators on the left hand side, from top to bottom, consist of a 32 MVA 1977 General Electric steam turbine, a 53.9 MVA 1986 Westinghouse gas fired turbine, and a 32 MVA 2004 Siemens combined cycle steam turbine.

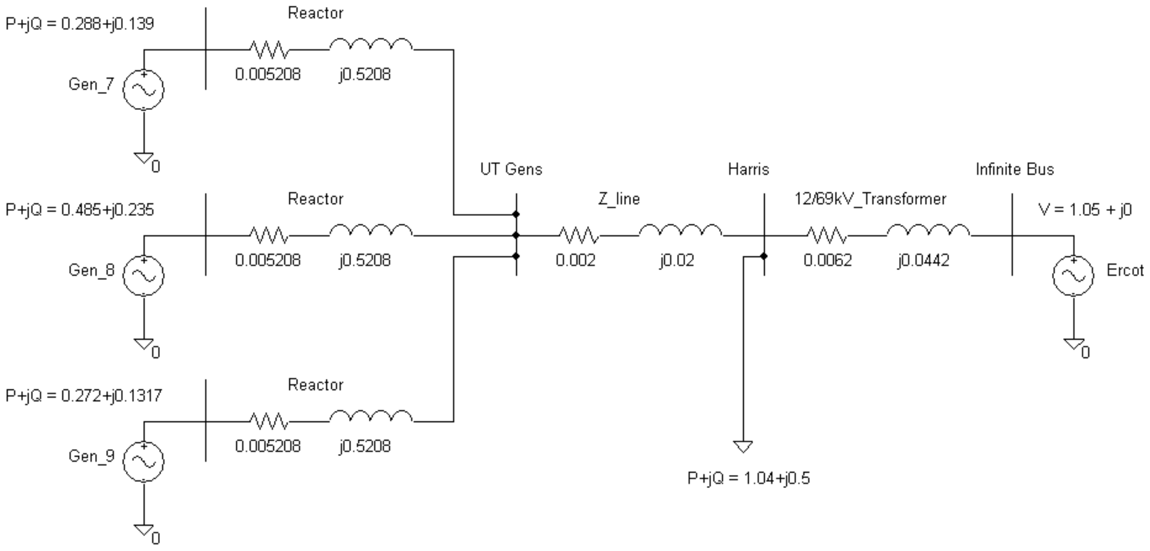


Figure 9.4. UT power system one-line diagram.

All values in Figure 9.4 are in per unit on 100 MVA base. The voltage base is 12 kV for UT and 69 kV for ERCOT. The load is rated at the maximum power capability for all three UT generators. The transformer impedance includes the Thevenin impedance of ERCOT seen from Harris Substation which is found with a short circuit analysis at the Harris Bus. On the right side of the transformer is the equivalent ERCOT system. The system parameters for ERCOT are assumed to have a high inertia due to the overall size and strength of the system, thus representing an infinite bus holding the system frequency constant.

9.3.1 PSS/E

9.3.1.1 System with reactors

Power System Simulator for Engineers (PSS/E) is a commercially available software package used to model large scale power systems. Highly detailed models for various generators, exciters, governors, transmission lines, and traditional loads are included with the software. The program can be used for load flow and dynamic simulation to study system transient response and stability.

The UT system is initially developed in PSS/E and the steady state load flow data has been included in Table 9.1. In the first dynamic simulation, various duration three-phase to ground faults are applied at the Harris bus. The exciter for Generator 8 is modeled for all three generators. As shown in Figure 9.5, the rotors for Generator 7, 8, and 9 swing for a six-cycle fault and then damp out. If the exciters are not included in the simulation and therefore a constant field voltage is assumed, the first swing rotor angles slightly increase. This can be seen in Figure 9.6. The exciters, however, have a more pronounced impact on the subsequent swings. All elements are important for the true system response; however, since I am interested in first swing transient stability, using a constant field voltage is adequate. The base-case system model uses line reactors and a constant field voltage.

Table 9.1. UT System Load Flow Data from PSS/E.

	V term	Θ term	MVA	E field
ERCOT	1.05	0.0	0.44+j21.74	1.246
Generator 7	1.107	8.515	28.8+j13.94	2.774
Generator 8	1.135	13.32	48.5+j23.49	3.224
Generator 9	1.104	8.119	27.2+j13.17	2.713

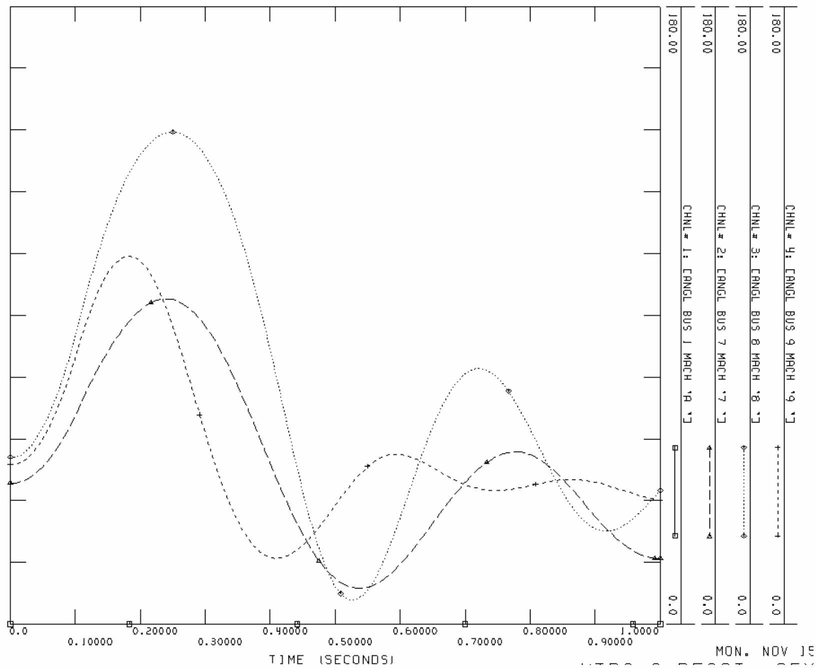


Figure 9.5. Generator rotor angles for UT system with reactors and exciters, fault = 0.1sec.

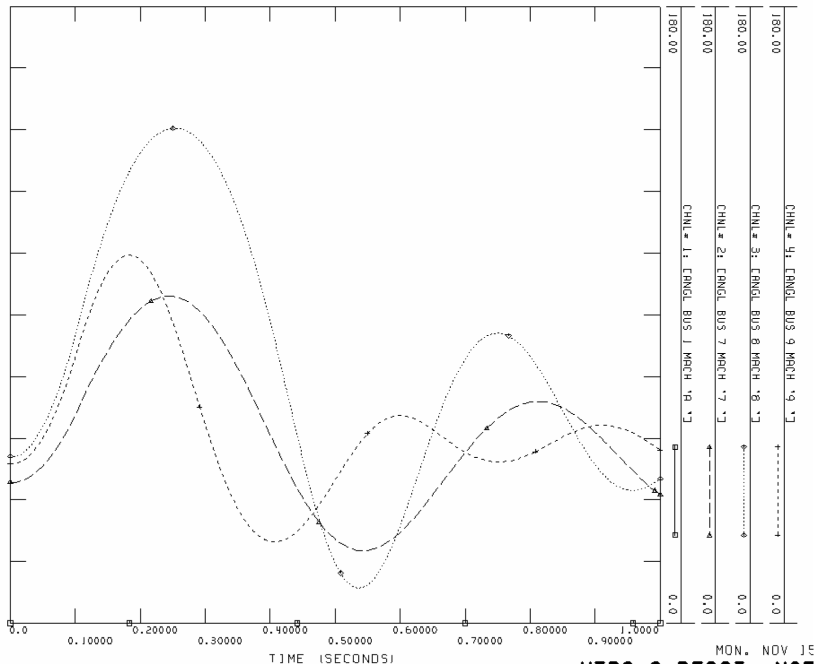


Figure 9.6. Generator rotor angles for UT system with reactors and no exciters, fault = 0.1sec.

The rotor angle response in Figure 9.7 is generated by increasing the fault to 6.5 cycles. At this time generator 8 is driven unstable. Continuing to increase the fault clearing time, generator 9 is the next to go unstable at 8 cycles followed by generator 7 at 8.5 cycles. The reactors reduce the short circuit current and isolate the generators from one another. The isolation allows the generators to have different critical clearing times.

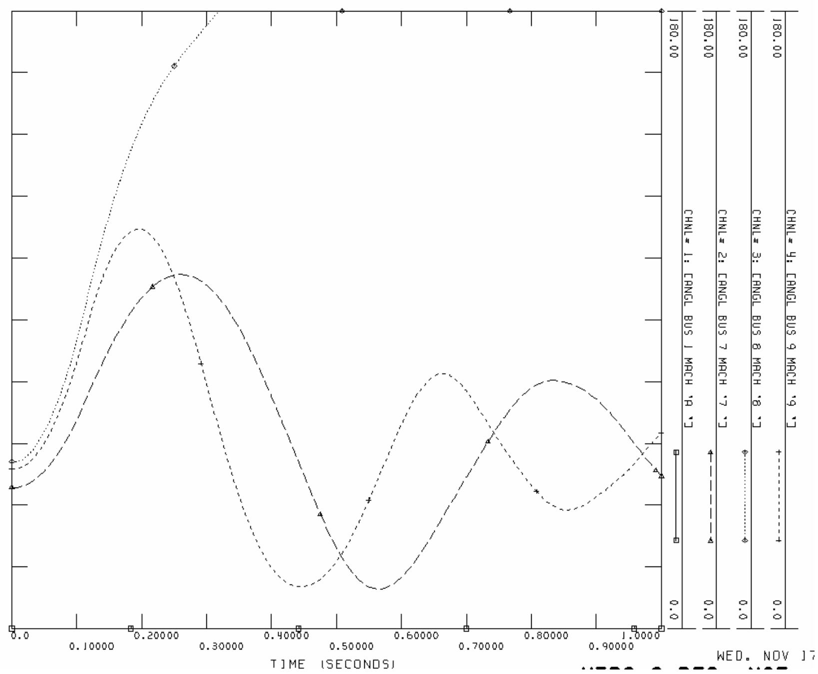


Figure 9.7. Generator rotor angles for UT system with reactors and no exciters, fault = 0.108sec.

9.3.1.2 System without Reactors

The six cycle fault response seen in Figure 9.8 is generated excluding the current limiting line reactors. The steady state power angles are less than when the reactors are included. The decrease in steady state rotor angles lead to a decrease in peak rotor angle swings, thus increasing the generators critical clearing times. Generator 8 does not go unstable until an 8.5 cycle fault. All three generators, however, are less isolated from one another without the reactors. This causes the other two generators to lose stability for a nine cycle fault.

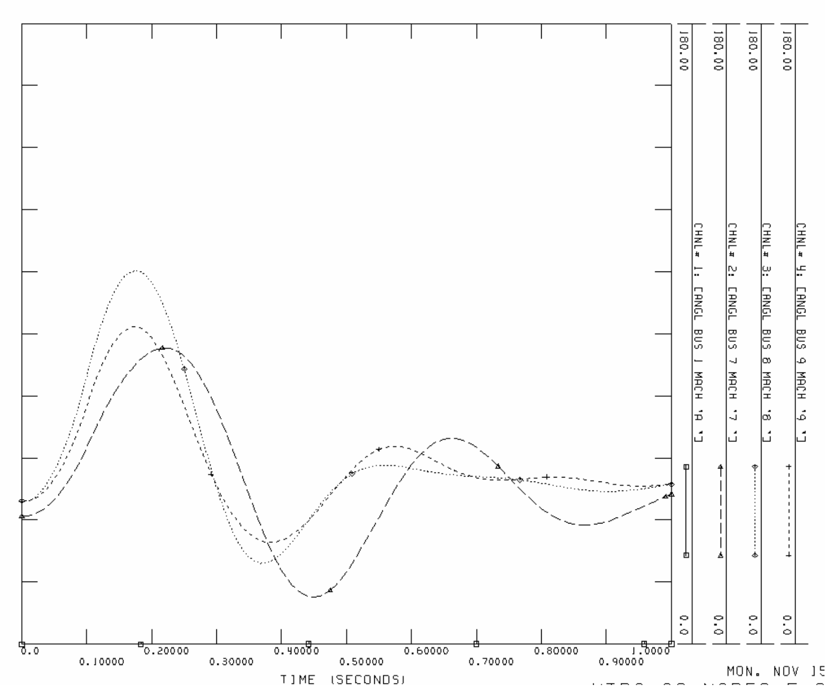


Figure 9.8. Generator rotor angles for UT system without reactors, fault = 0.1sec.

9.3.2 Equal Area Criterion

The EAC is used to check the PSS/E stability results. A three-phase line to ground fault occurring and the Harris bus would collapse the voltage and entire load demand. This causes the fault electrical power curve of the generator to go to zero. After the fault is cleared, the system operating conditions are the same as before the fault occurred. The corresponding EAC is shown in Figure 9.9.

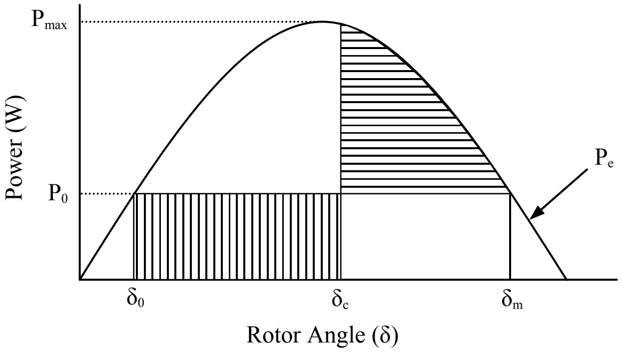


Figure 9.9. EAC power-angle curve for UT power system.

The critical clearing angle can be determined by equating the kinetic energy gained by the rotor during the fault (vertically shaded region) to the energy lost after the fault is cleared (horizontally shaded region). Knowing the steady state rotor angle δ_o and the corresponding angle δ_m the critical clearing angle δ_{cl} can be solved by

$$\delta_{cl} = \cos^{-1}\left(\frac{P_0 \cdot (180 - 2 \cdot \delta_0) \cdot \pi}{180 \cdot P_{\max}} + \cos(180 - \delta_0)\right) \tag{9-10}$$

where $P_{\max} = \frac{\left|E_a'\right| \cdot \left|V_L\right|}{X_T}$, δ is in degrees, and all other variables are defined in (9-8). Integrating the swing equation

$$\frac{2H}{\omega}\frac{d^2\delta(t)}{dt^2} = P_0 \tag{9-11}$$

twice with $\delta(0) = \delta_0$ and $\frac{d\delta(0)}{dt} = 0$, the critical clearing time t_{cl} can be solved as

$$t_{cl} = \sqrt{\frac{4H \cdot}{\omega \cdot P_0}(\delta_{cl} - \delta_0)\frac{2\pi}{360}}\ . \tag{9-12}$$

Variable H is the inertia constant of the synchronous machine.

Although the EAC is not intended to be used for multi-machine stability, the reactors isolate the generators from one another and allow the generators to be treated independently. Solving these equations with the steady state load flow data shown in Table 9.1 for the UT system, the solutions match favorably to those provided through the dynamic stability simulations in PSS/E. The critical clear times are shown in Table 9.2.

The EAC critical clearing times are overestimated due to the dynamics of the multi-machine system that are not included in the analysis.

Table 9.2. UT System Critical Clearing Times (sec).

	PSS/E	Equal Area Criterion	Numerical Stability	Simulink
Generator 7	0.146	0.198	0.179	0.164
Generator 8	0.104	0.128	0.121	0.118
Generator 9	0.129	0.163	0.146	0.146

9.3.3 Numerical Stability

Explicit numerical integration can also be used to solve system stability using the swing equation. The mechanical power to the generator during the fault accelerates the generator based the machines inertia. When the electrical power output during the fault is zero, the acceleration is constant, the machines velocity changes linearly, and the angular change is quadratic.

When the fault clears, the electrical output power increases beyond the mechanical power input and begins to decelerate the generator. Kinetic energy stored in the rotor is absorbed by the system. The generator responses for a 7.5 cycle fault are given in Figure 9.10. The critical clearing times are included in Table 9.2. These results are similar to the EAC. This analysis does not include the multi-machine dynamics and therefore the critical clearing times are overestimated.

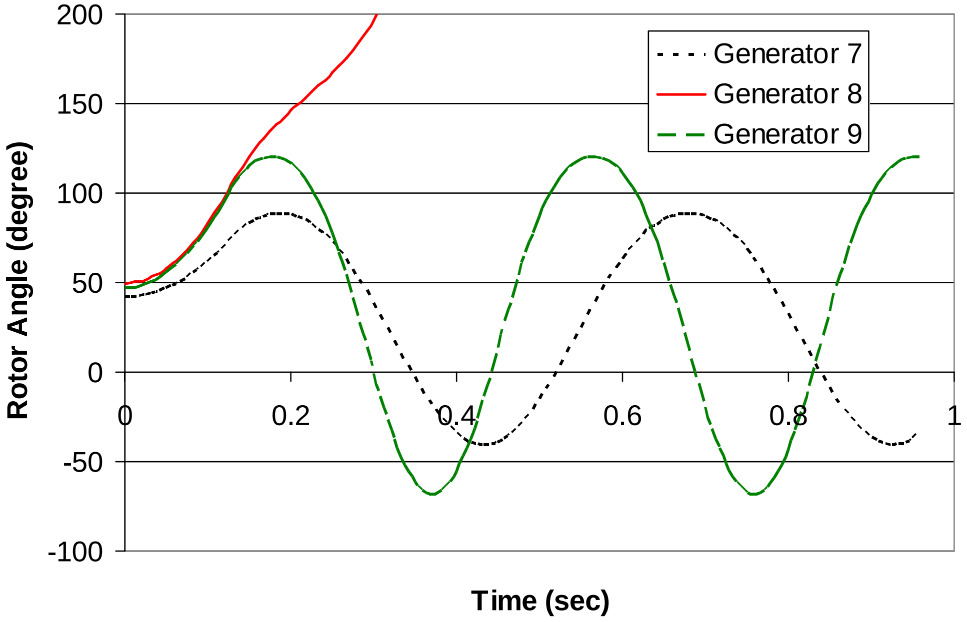


Figure 9.10. Numerical stability for UT system showing generator 8 instability at 0.125seconds.

9.3.4 Simulink

The power systems toolbox in Matlab/Simulink is used to reconstruct the UT power system. Simulink is chosen because user defined models are less complicated to implement. Due to differences between Simulink and PSS/E, the stability results are slightly different. The Simulink steady state load flow data is included in Table 9.3 and matches the PSS/E load flow data from Table 9.1. As shown in Table 9.2, the critical clearing times determined in Simulink are approximately one cycle longer than those of PSS/E yet shorter than the EAC and Numerical Stability results. Simulink models are not as advanced as PSS/E yet the dynamics are similar enough to make my analyses.

Table 9.3. UT System Load Flow Data from Simulink.

	V term	Θ term	MVA	E field
ERCOT	1.05	0.0	3.3+j24.5	1.092
Generator 7	1.106	8.39	28.8+j13.9	2.58
Generator 8	1.135	13.15	48.5+j23.5	2.746
Generator 9	1.103	7.94	27.0+j13.1	2.259

9.3.4.1 Critical Clearing Times

To determine the most significant impact of the power electronic load, the complete active power load (104MW) is replaced by the power electronic model developed in Chapter 5. In the worse case scenario (i.e., three-phase to ground fault at the Harris bus), the bus voltage collapses to zero. This causes the load to effectively trip off during the complete fault (i.e., $P_f(t)=0$). Under the assumption that the power electronic load capacitors discharge completely during the fault and do not automatically shut down, the power electronic load will demand the discharged energy

$$E_2 = P \cdot \Delta t \leq \frac{1}{2} C \cdot V^2 \qquad (9\text{-}13)$$

after the fault clears. The post-fault time constant for the utility power electronic load in Chapter 8 is 0.02 seconds for approximately 10% of total MW load. As the load increases and the fault voltage goes to zero, the post-fault time constant will only slightly change. A 0.03 second and 0.05 second time constant have been selected.

The critical clearing times from Simulink using the tradition dynamic load are repeated in Table 9.4. These clearing times are compared to the critical clearing times if the active power portion of the traditional load is replaced with a power electronic load. The first observation made is the impact of the power electronic load if there is no post-fault response. This response resembles a power electronic load with a shut-down setting when the fault occurs (i.e., V_{trip} = 0.99Vpu). Therefore, the power electronic load capacitors would not discharge energy during the fault. No post-fault response demands approximately the same power in the post-fault as the traditional dynamic load. The clearing times when using the power electronic load with no post-fault response are given in Table 9.4. These clearing times are slightly shorter than those when using the traditional load. Because generator 8 trips 2ms earlier, there is a cascading effect that causes generator 9 to trip 3ms sooner and then generator 7 to trip 7ms earlier than in the traditional load case.

Table 9.4. UT System Critical Clearing Times (sec) from Simulink.

	Traditional Dynamic Load	Power Electronic: No PF Inrush	Power Electronic: $\tau_{pf} = 0.05$	Power Electronic: $\tau_{pf} = 0.03$
Generator 7	0.164	0.157	0.151	0.149
Generator 8	0.118	0.116	0.107	0.106
Generator 9	0.146	0.143	0.135	0.132

Assuming the load does not shut-down in the fault (i.e., V_{trip} = 0.0Vpu), a 0.77nF/W storage factor, and a 10kV pre-fault steady state capacitor voltage, the composite power electronic load capacitor voltage decays to zero if the fault lasts 0.077sec. Any fault lasting longer than 0.077sec demands no more energy than required to recharge the composite capacitor completely back to steady state. In this case, the post-fault energy E_2 is

$$E_2 = P \cdot \Delta t \leq \frac{1}{2} C V^2 = \frac{1}{2}\left(1.54 \frac{nF}{W} \cdot 104 MW\right) 10000^2 = 8 MJ \, . \qquad (9\text{-}14)$$

The post-fault inrush of the power electronic load decreases the critical clearing times as shown in Table 9.4. As the post-fault inrush magnitude increases for a shorter time constant, the critical clearing times decrease further.

9.3.4.2 *Three Cycle Fault*

Unlike the results for the previous section, the post-fault inrush of the power electronic load improves the rotor angle swing for short duration faults. Table 9.5 shows the change in rotor angle for each generator when the fault is cleared after three cycles. For the short fault, the additional post-fault power inrush increases the generator decelerating forces and decreases the rotor angle swings. When the fault increases to the critical clearing time as in the previous section, the post-fault inrush further aggravates the system causing the system energy absorbing capability to decrease further than the increase in post-fault power. This is explained further in the 9.4.1.1.

Table 9.5. UT System Generator Rotor Angle Swing (degree) from Simulink for three cycle fault.

	Traditional Dynamic Load	Power Electronic: No PF Inrush	Power Electronic: $\tau_{pf} = 0.05$	Power Electronic: $\tau_{pf} = 0.03$
Generator 7	18.9	16.9	12.6	11.7
Generator 8	29.3	28.1	25.2	24.5
Generator 9	18.3	16.9	13.7	12.9

9.3.4.3 *Actual DBR Response*

To further validate the power electronic load model, the model is replaced by an actual switching DBR circuit in the transient simulation. As shown in Table 9.6 for the three cycle fault, the post-fault inrush when using the DBR load causes the rotor of each generator to swing less than when the linear load model is used and greater than when the power electronic load model is used. When the fault is increased to six cycles, which is near the critical clearing time for generator 8 and 9, the rotor swing for the DBR load is greater than when the linear load is used. Thus, as the power electronic model predicted, there is a decrease in critical clearing time for the actual power electronic load when the inrush occurs near the critical clearing time.

Table 9.6. UT System Generator Rotor Angle Swing (degree) from Simulink using actual DBR model.

		Traditional Dynamic Load	Power Electronic: DBR Load	Power Electronic: $\tau_{pf} = 0.05$	Power Electronic: $\tau_{pf} = 0.03$
3 Cycle Fault	Gen 7	18.9	13.5	12.6	11.7
	Gen 8	29.3	27	25.2	24.5
	Gen 9	18.3	16	13.7	12.9
6 Cycle Fault	Gen 7	45.2	39.7	36.8	34.3
	Gen 8	75.7	92.4	76.2	80.2
	Gen 9	51.3	51.4	46.9	45.8

Discrepancies between the DBR results and the power electronic transient load model results are due to differences in the post-fault inrush power. The power electronic model assumes the system voltage returns to nominal quickly after the fault clears and the inrush power charges the load capacitor back to steady state. In the simulation with the DBR load, however, the capacitor charges more slowly because the system voltage takes longer to return to the nominal value. Thus, results in a longer post-fault time constant. The impact of the power electronic model closely matches, yet is slightly different, than the actual DBR load.

9.4 SIMULINK ONE MACHINE INFINITE BUS (GEN 7 AND 8 DISCONNECTED)

9.4.1 Load and Fault at Harris Bus

The steady state load flow data are shown in Table 9.7 when the load is at the Harris bus and generator 7 and 8 are disconnected. The Harris bus load is reduced to the maximum power capability of Generator 9.

Table 9.7. Generator 9/Infinite Bus Load Flow Data from Simulink.

	V term	Θ term	MVA	E field
ERCOT	1.05	0.0	1.95+j4.16	1.057
Generator 9	1.107	7.14	27.2+j13.7	2.485

Table 9.8 shows the critical clearing times for a fault occurring at the Harris bus for several system and load variations. The simulated critical clearing time is 0.166sec for the traditional load and 0.167sec for the power electronic load with no post-fault response. As expected, these results are similar.

Table 9.8. Generator 9/Infinite Bus Critical Clearing Times (sec) from Simulink.

	Generator 9
Traditional Dynamic Load	0.166
Power Electronic: No PF Response	0.167
Power Electronic: $\tau_{pf} = 0.03$	0.162
Power Electronic: $\tau_{pf} = 0.03$, Load trip at 50% voltage	0.165
Power Electronic: No PF Response, Exciter & Governor	0.174
Power Electronic: $\tau_{pf} = 0.03$, Exciter & Governor	0.170

The critical clearing time is influenced by the magnitude of power demanded immediately following the fault. The critical clearing time reduces to 0.162sec when the load has a post-fault transient assuming all energy has been discharged from the capacitors. If the load shuts-down when the power electronic capacitor voltage reaches approximately 50% in the fault (i.e., $V_{trip} = 0.5Vpu$), the total energy displaced from the capacitors and therefore initial post-fault inrush would decrease. This causes the critical clearing time to be 0.165sec. The critical clearing time is dependent on the magnitude of the post-fault inrush.

The overall critical clearing times increase when including a default exciter and governor. However, the power electronic post-fault inrush still decreases the critical clearing times as shown in Table 9.9.

Table 9.9. Generator 9/Infinite Bus Critical Clearing Times (sec) from Simulink when Exciter and Governor are Included.

	Generator 9
Power Electronic: No PF Response	0.174
Power Electronic: $\tau_{pf} = 0.03$	0.170

9.4.1.1 Decrease in UEP and PEBS

The critical energy demanded after a severe fault where the power electronic load completely disconnects increases by

$$W_{cr,load} = P \cdot \left(t_{cl} - t_{SEP}\right) \leq \frac{1}{2} C \cdot V^2 . \qquad (9\text{-}15)$$

An increase in critical energy corresponds to an increase in stability by Lyaponov's energy analysis. However, the contrary is true. Figure 9.11a shows the positive sequence voltage for no post-fault response while Figure 9.11b is when there is a post-fault inrush. The post-fault voltage in Figure 9.11a is slightly higher than that of Figure 9.11b. The inrush current to the power electronic load causes a greater voltage drop and therefore decreases the system voltage.

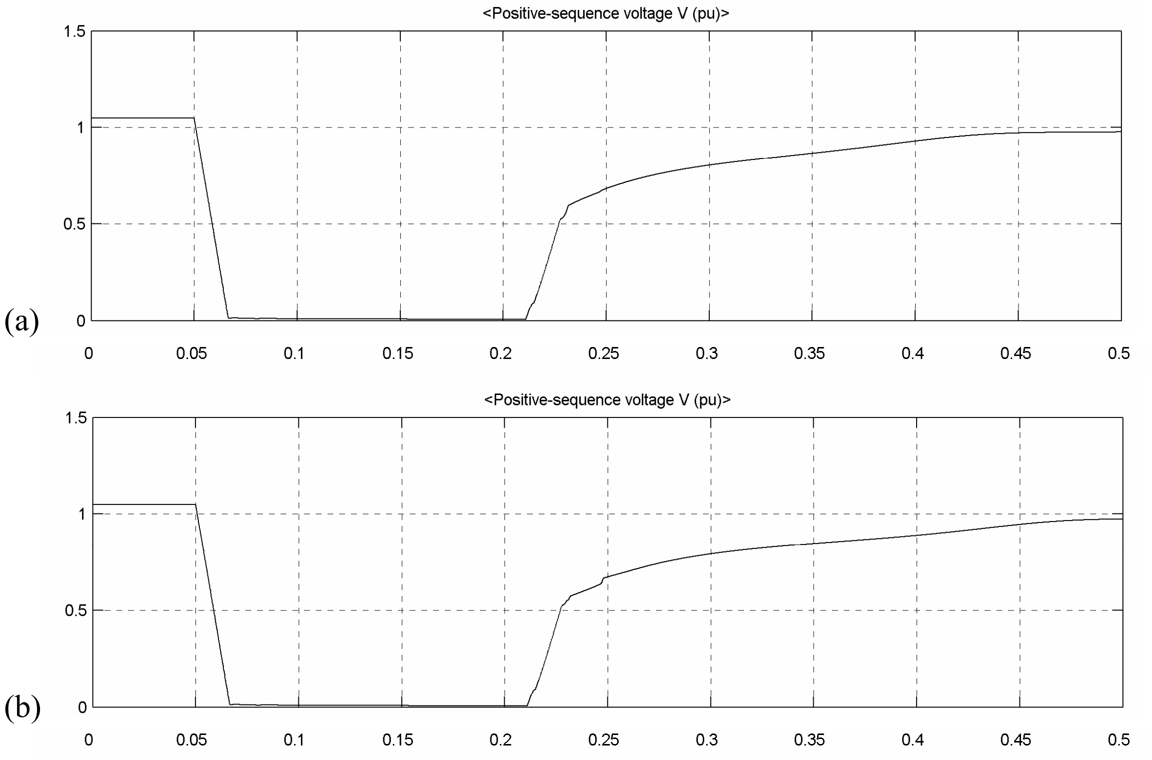


Figure 9.11. Positive sequence load voltage (a) without post-fault inrush and (b) with post-fault inrush.

The decrease in system voltage during the post-fault inrush affects the power-angle curve immediately following the fault. The maximum power P_{max} decreases which leads to a decrease in the angle of the UEP as shown in Figure 9.12. For example, when the power electronic load has no post-fault response, the angle of the unstable equilibrium point is 128 degrees whereas the angle is 121 degrees with the post-fault response.

Overall, the potential energy that the system can absorb decreases greater than the additional energy demanded by the power electronic load. The net effect is the PEBS decreases and therefore leads to a decrease in stability margin.

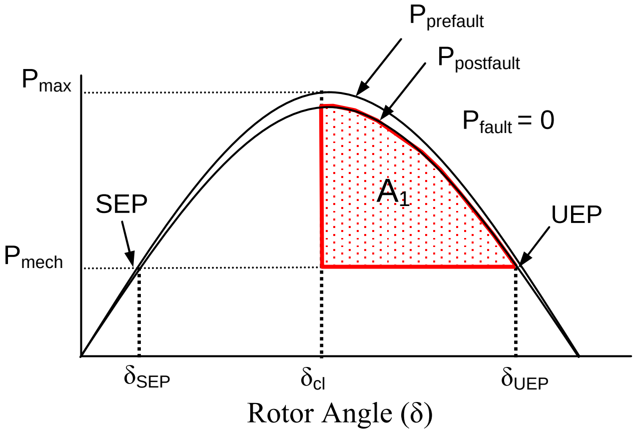


Figure 9.12. Power-angle curve representing decrease in P_{max} and UEP.

9.4.2 Load Near Generator and Fault at Harris Bus

The location of the load is important to the generator transient response. When the fault is at the Harris bus and the load is located near the generator, the load voltage does not collapse to zero. This allows the load to come back online during the fault. The characteristics for the utility load in Chapter 8 show the fault response shape is near one (exponential) with a time constant close to 0.05sec. Using fault time constant λ = 0.06sec, shape $k = 1.2$, and post-fault time constant $\tau_{pf} = 0.03$sec, the load and generator response are shown in Figure 9.13. At the beginning of the fault, there is no load, but by the end of the fault, the load is almost back to steady state power.

The generator response is significantly different with a conventional linear load. The response for a constant impedance linear load is given in Figure 9.14 followed by the response for a constant power linear load in Figure 9.15. The constant impedance load causes the generator rotor to swing the greatest; the constant power load reduces the rotor swing; and the power electronic load improves the rotor swing the most.

The net impact is that the dynamics of the power electronic load is beneficial to the system when the load comes online during a fault. The momentary decrease in load allows the generator to accelerate; however, the increase in load with the depressed load voltage causes a significant increase in generator current which promptly decelerates the generator. The post-fault inrush is limited because the load capacitor is not completely discharged. The rotor swing damps out fast.

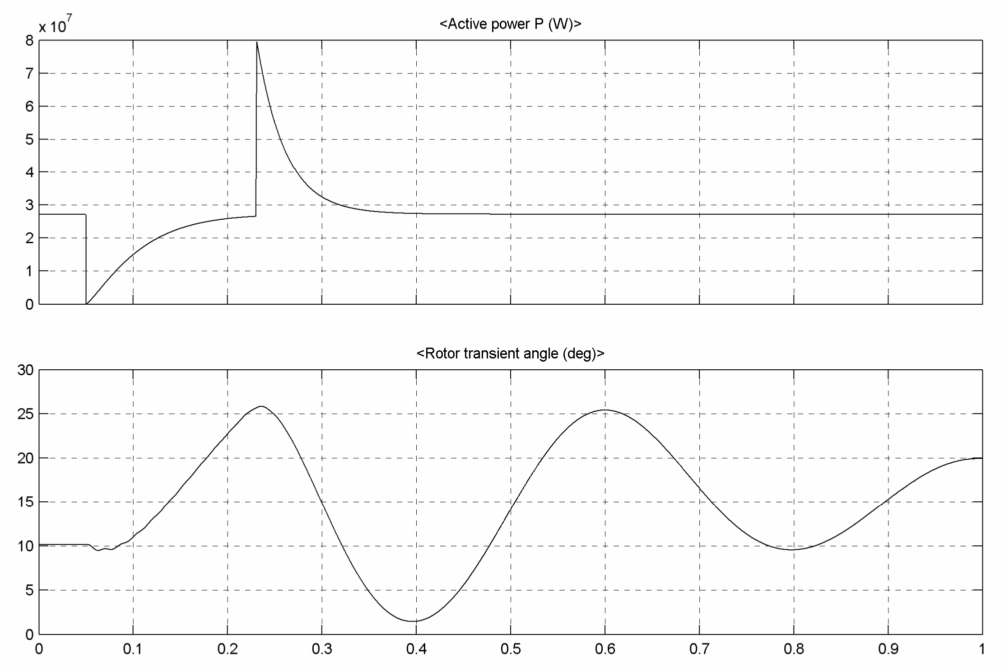


Figure 9.13. System response for power electronic load.

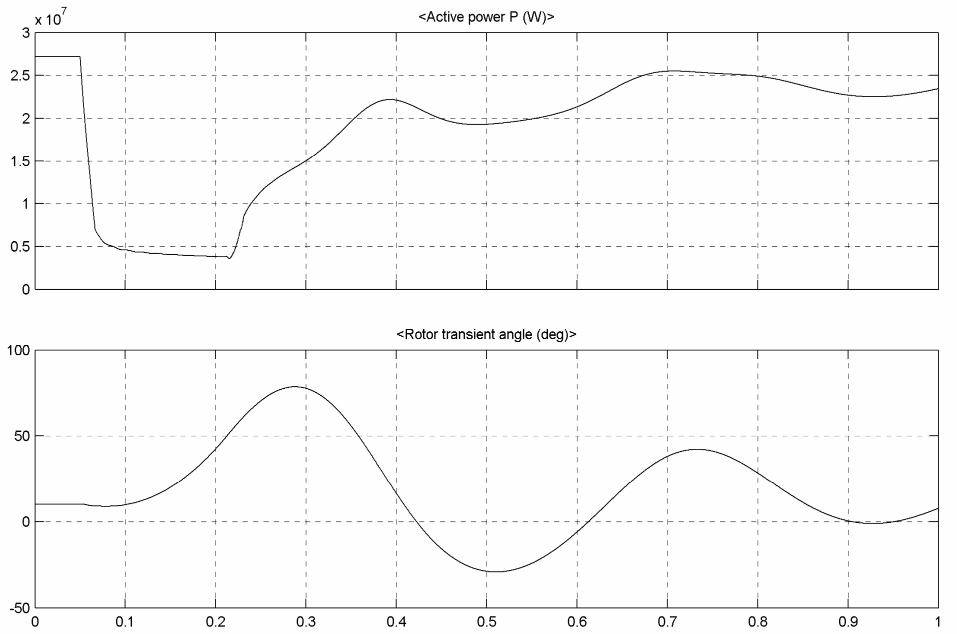


Figure 9.14. System response for constant impedance linear load.

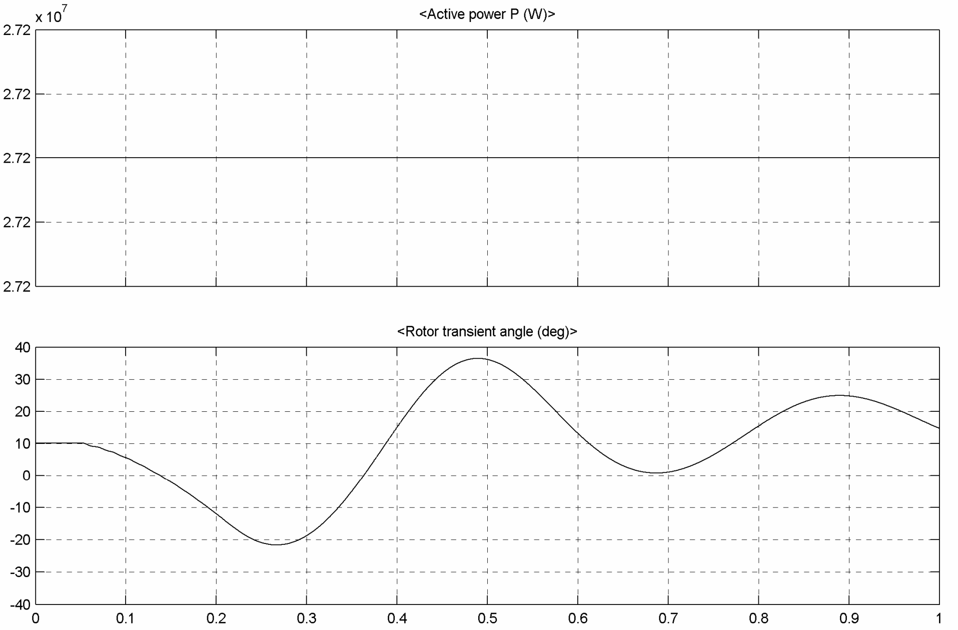
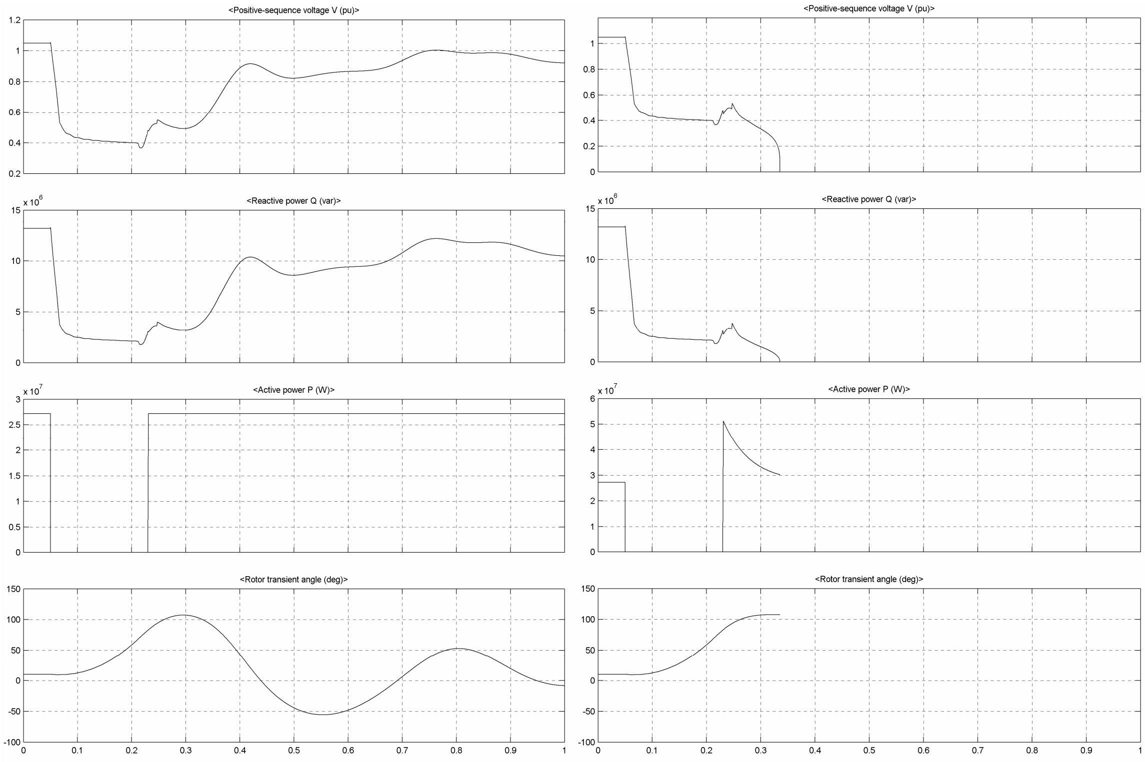


Figure 9.15. System response for constant power linear load.

If the load had not come back online in the fault due to a low voltage load shut-down, the rotor accelerates faster than with the constant impedance load. The post-fault inrush would occur demanding the energy depleted to the voltage shut-down level V_{trip}. Figure 9.16a shows the system response returns to a SEP if the load had shut-down before any energy had been depleted (i.e., V_{trip} = 0.99pu). If the load had shut-down after the capacitors discharged to 0.5Vpu, there would be a post-fault transient with the response shown in Figure 9.16b. The shut-down followed by the post-fault response near the accelerating machine decreases the stability margin and leads to a voltage collapse.



(a) (b)

Figure 9.16. System response to power electronic load trip at (a) 0.99Vpu and (b) 0.5Vpu.

9.5 POWER ELECTRONIC LOAD TRANSIENT ENERGY FUNCTIONS

The power electronic load decreases the clearing energy W_{cl} by

$$W_{cl,load} = \int_{T_f}^{T_{cl}} \left(P_{onset} + \left(P_0 - P_{onset}\right) \cdot \left(1 - \exp\left(- \left(\frac{t - T_f}{\lambda} \right)^k \right) \right) \right) dt \qquad (9\text{-}16)$$

where T_{cl} is the clearing time and T_f is the onset time of the fault.

The critical energy W_{cr} increases by

$$W_{cr,load} = \int_{T_{cl}}^{T_{UEP}} \left(P_0 + \left(\frac{P_0 \cdot \left(T_{cl} - T_f\right) - W_{cl,load}}{\tau_{pf}} \right) \cdot \exp\left(- \left(\frac{t - T_{cl}}{\tau_{pf}} \right) \right) \right) dt \qquad (9\text{-}17)$$

The time of the UEP T_{UEP} has been observed to be reached approximately 0.12sec after the fault is cleared. Based on this length of time, the post-fault inrush, with $\tau_{pf} = 0.03$sec, has decayed back to steady state. Therefore, the increase in critical energy reduces to

$$W_{cr,load} = P_0 \cdot \left(T_{cl} - T_f\right) - W_{cl,load} + \int_{T_{cl}}^{T_{UEP}} P_0 dt \le \frac{1}{2} C \cdot V^2 + \int_{T_{cl}}^{T_{UEP}} P_0 dt \,. \qquad (9\text{-}18)$$

9.6 SUMMARY

The power electronic load fault response has a significant impact on the system transient response. As long as the load can reconnect to the system in the fault without further depressing the system voltage, the generator rotor swings less than when the traditional linear load is used. The load reconnecting also limits the post-fault inrush. If the load, however, does not come back online in the fault, the rotor swings further than when the traditional load is used. Power electronic load reconnecting to the system in the fault improves the system transient response.

The power electronic load post-fault inrush increases the generator decelerating forces and improves the rotor swing for short duration faults. However, when the fault persists near the critical clearing time, the system is further aggravated by the post-fault inrush causing a decrease in system voltage and unstable equilibrium point. The post-fault inrush slightly decreases the critical clearing times because the additional energy drawn by the load is less than the reduction in the system energy absorbing capability. For the UT three generator example, the critical clearing times decrease by approximately 10msec.

Summarizing, the power electronic load can have a friendly or unfriendly affect on the system transient response and stability depending on the location of the load and the type, location, and duration of the fault. To minimize the power system transient response,

- the load should come back online in the fault, and
- the post-fault inrush should be limited.

To prevent the load from shutting-down in the fault, a reduced low-voltage trip level must be applied. To limit the post-fault inrush, the post-fault time constant must increase, or the energy dissipated in the fault must be minimized. Since minimizing the energy dissipated in the fault requires the load to shut-down instead of attempting to ride-through the fault, increasing the time constant is preferred. To increase the time constant, one option is current limiting reactors, and another option is increasing the time that the system voltage takes to return to steady state after the fault is cleared.

The power electronic transient load model is best suited for the case when the system voltage is known at the onset of the fault and the system voltage returns to nominal at fault clearing. The switching model equations (5-4), (5-5), and (5-7) take into consideration the dynamic system voltage, however only represent the average load. Since the power electronic load affects the system transient response and stability, one of these models should be included in system studies.

Chapter 10 – Conclusion

The transient response of power electronic loads is considerably different than traditional loads, and therefore, a new transient load model has been developed. The load model is based on the average system power drawn over a 60Hz cycle. The load recovery during the fault is well represented as a Weibull CDF whose response is dependent on the distribution shape and the fault time constant. The post-fault transient is an Exponential PDF whose response is dependent on the energy dissipated from the power electronic load DC capacitor during the fault and the post-fault time constant.

From the simulated response data, fault time constant λ, fault shape k, and post-fault time constant τ_{pf} are dependent on system impedance, load capacitance, load power, and fault voltage. Characteristics k and λ are governed by the storage factor ride-through time. For the average load with a storage factor allowing 5% voltage ripple, λ is approximately 0.04sec, k is approximately 1.1, and the post-fault time constant is approximately 0.02sec.

The power electronic load model has been validated with the actual voltage sag response of laboratory controlled loads. The composite load model transient characteristics are determined using the known model parameters and the analytical dynamic equations. The simulated and actual responses compare favorably.

The residential utility power electronic load is often 10-15% of the total MW demand. The observed utility power electronic load fault response shape is close to 1.1 with a 0.04sec time constant. The post-fault response has a 0.015sec time constant.

In a transient stability study of the University of Texas at Austin power system, the entire active power load is replaced with the power electronic load model. The characteristics of the power electronic load are similar to those on the utility feeder. The response of the power electronic load is friendly to power system transient response when located near accelerating machines assuming the load comes back online in the fault. For short duration faults where the load does not reconnect to the system in the fault, the post-fault inrush decelerates the generator and also improves the generator transient response. As the fault duration increases toward the critical clearing time, however, the post-fault inrush further aggravates the system and decreases the stability margin.

The power electronic load can be friendly or unfriendly to power system transient response and stability, and therefore, should be included in system stability studies.

In summary, the main contributions of this dissertation are

1. A measurement-based procedure to
    - determine the amount of composite power electronic load on distribution feeders, and
    - determine the stability load model characteristics for traditional linear loads
2. A transient model for composite single-phase power electronic loads that is suitable for incorporation into transient stability studies of electric power grids.
3. Transient load model validated with
    - laboratory load using Voltage Sag-Test Station, and
    - actual utility load using naturally occurring events.
4. Recommended load modeling characteristics using simulated load response.
5. Evaluation of the impact of power electronic loads on power system transient response and stability.

Additional contributions of the dissertation are

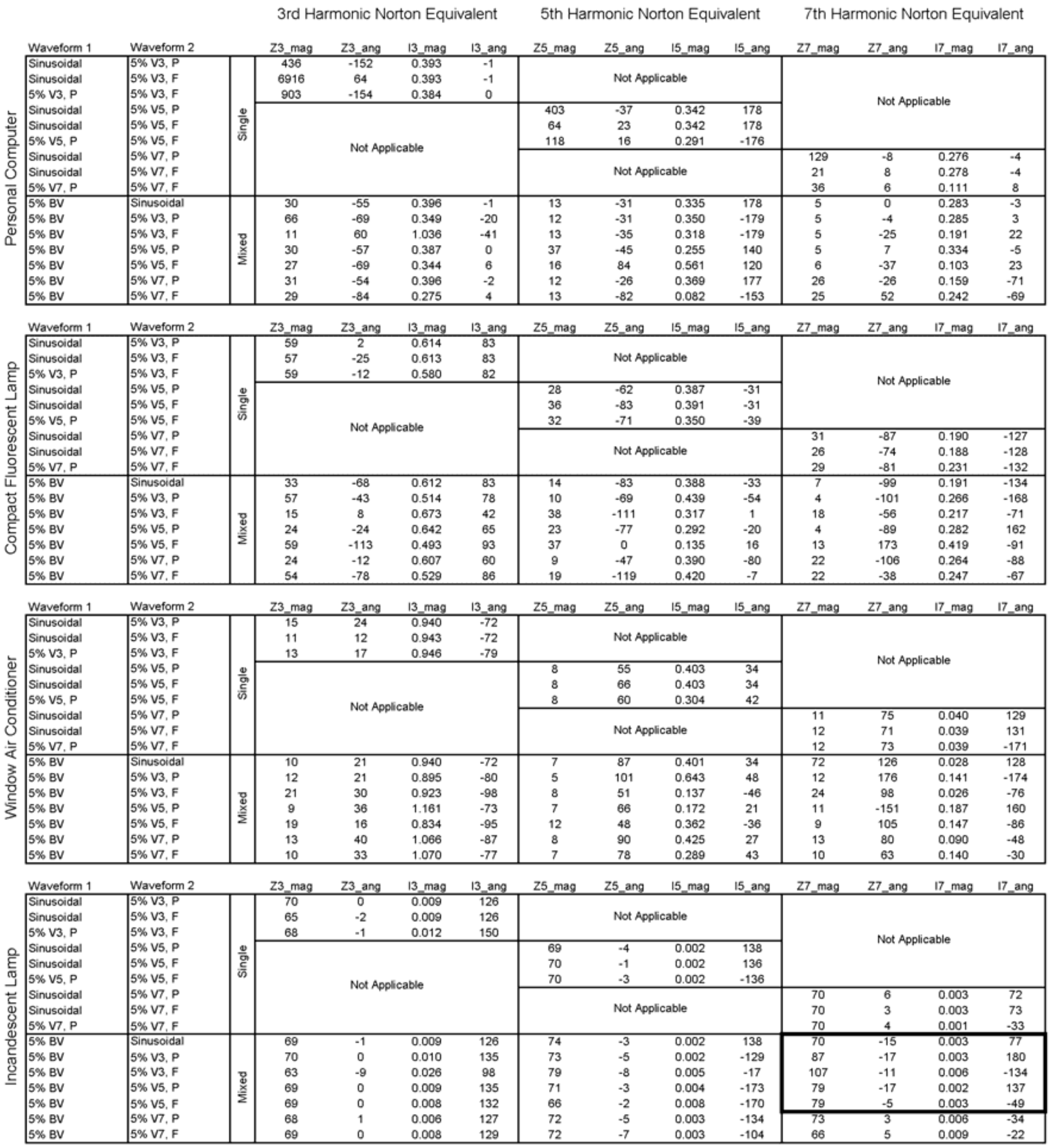
6. The development of a harmonics testing station to

- examine the relationship between voltage and current distortion of power electronic loads, and
- provide a careful examination and identification of the serious errors associated with the use of Norton equivalents for power electronic loads.

7. The development of a system impedance monitoring station which uses the power electronic load to
    - measure system impedance and
    - identify system resonance.

Appendices

APPENDIX A – COMPLETE SET OF NORTON LOAD MODEL RESULTS (SINE ANGLES)



				3rd Harmonic Norton Equivalent				5th Harmonic Norton Equivalent				7th Harmonic Norton Equivalent			
	Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang	Z5_mag	Z5_ang	I5_mag	I5_ang	Z7_mag	Z7_ang	I7_mag	I7_ang
Personal Computer	Sinusoidal	5% V3, P	Single	436	-152	0.393	-1	Not Applicable				Not Applicable			
	Sinusoidal	5% V3, F		6916	64	0.393	-1								
	5% V3, P	5% V3, F		903	-154	0.384	0								
	Sinusoidal	5% V5, P		Not Applicable				403	-37	0.342	178				
	Sinusoidal	5% V5, F						64	23	0.342	178				
	5% V5, P	5% V5, F						118	16	0.291	-176				
	Sinusoidal	5% V7, P						Not Applicable				129	-8	0.276	-4
	Sinusoidal	5% V7, F										21	8	0.278	-4
	5% V7, P	5% V7, F										36	6	0.111	8
	5% BV	Sinusoidal	Mixed	30	-55	0.396	-1	13	-31	0.335	178	5	0	0.283	-3
	5% BV	5% V3, P		66	-69	0.349	-20	12	-31	0.350	-179	5	-4	0.285	3
	5% BV	5% V3, F		11	60	1.036	-41	13	-35	0.318	-179	5	-25	0.191	22
	5% BV	5% V5, P		30	-57	0.387	0	37	-45	0.255	140	5	7	0.334	-5
	5% BV	5% V5, F		27	-69	0.344	6	16	84	0.561	120	6	-37	0.103	23
	5% BV	5% V7, P		31	-54	0.396	-2	12	-26	0.369	177	26	-26	0.159	-71
	5% BV	5% V7, F		29	-84	0.275	4	13	-82	0.082	-153	25	52	0.242	-69

	Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang	Z5_mag	Z5_ang	I5_mag	I5_ang	Z7_mag	Z7_ang	I7_mag	I7_ang
Compact Fluorescent Lamp	Sinusoidal	5% V3, P	Single	59	2	0.614	83	Not Applicable				Not Applicable			
	Sinusoidal	5% V3, F		57	-25	0.613	83								
	5% V3, P	5% V3, F		59	-12	0.580	82								
	Sinusoidal	5% V5, P		Not Applicable				28	-62	0.387	-31				
	Sinusoidal	5% V5, F						36	-83	0.391	-31				
	5% V5, P	5% V5, F						32	-71	0.350	-39				
	Sinusoidal	5% V7, P						Not Applicable				31	-87	0.190	-127
	Sinusoidal	5% V7, F										26	-74	0.188	-128
	5% V7, P	5% V7, F										29	-81	0.231	-132
	5% BV	Sinusoidal	Mixed	33	-68	0.612	83	14	-83	0.388	-33	7	-99	0.191	-134
	5% BV	5% V3, P		57	-43	0.514	78	10	-69	0.439	-54	4	-101	0.266	-168
	5% BV	5% V3, F		15	8	0.673	42	38	-111	0.317	1	18	-56	0.217	-71
	5% BV	5% V5, P		24	-24	0.642	65	23	-77	0.292	-20	4	-89	0.282	162
	5% BV	5% V5, F		59	-113	0.493	93	37	0	0.135	16	13	173	0.419	-91
	5% BV	5% V7, P		24	-12	0.607	60	9	-47	0.390	-80	22	-106	0.264	-88
	5% BV	5% V7, F		54	-78	0.529	86	19	-119	0.420	-7	22	-38	0.247	-67

	Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang	Z5_mag	Z5_ang	I5_mag	I5_ang	Z7_mag	Z7_ang	I7_mag	I7_ang
Window Air Conditioner	Sinusoidal	5% V3, P	Single	15	24	0.940	-72	Not Applicable				Not Applicable			
	Sinusoidal	5% V3, F		11	12	0.943	-72								
	5% V3, P	5% V3, F		13	17	0.946	-79								
	Sinusoidal	5% V5, P		Not Applicable				8	55	0.403	34				
	Sinusoidal	5% V5, F						8	66	0.403	34				
	5% V5, P	5% V5, F						8	60	0.304	42				
	Sinusoidal	5% V7, P						Not Applicable				11	75	0.040	129
	Sinusoidal	5% V7, F										12	71	0.039	131
	5% V7, P	5% V7, F										12	73	0.039	-171
	5% BV	Sinusoidal	Mixed	10	21	0.940	-72	7	87	0.401	34	72	126	0.028	128
	5% BV	5% V3, P		12	21	0.895	-80	5	101	0.643	48	12	176	0.141	-174
	5% BV	5% V3, F		21	30	0.923	-98	8	51	0.137	-46	24	98	0.026	-76
	5% BV	5% V5, P		9	36	1.161	-73	7	66	0.172	21	11	-151	0.187	160
	5% BV	5% V5, F		19	16	0.834	-95	12	48	0.362	-36	9	105	0.147	-86
	5% BV	5% V7, P		13	40	1.066	-87	8	90	0.425	27	13	80	0.090	-48
	5% BV	5% V7, F		10	33	1.070	-77	7	78	0.289	43	10	63	0.140	-30

	Waveform 1	Waveform 2		Z3_mag	Z3_ang	I3_mag	I3_ang	Z5_mag	Z5_ang	I5_mag	I5_ang	Z7_mag	Z7_ang	I7_mag	I7_ang
Incandescent Lamp	Sinusoidal	5% V3, P	Single	70	0	0.009	126	Not Applicable				Not Applicable			
	Sinusoidal	5% V3, F		65	-2	0.009	126								
	5% V3, P	5% V3, F		68	-1	0.012	150								
	Sinusoidal	5% V5, P		Not Applicable				69	-4	0.002	138				
	Sinusoidal	5% V5, F						70	-1	0.002	136				
	5% V5, P	5% V5, F						70	-3	0.002	-136				
	Sinusoidal	5% V7, P						Not Applicable				70	6	0.003	72
	Sinusoidal	5% V7, F										70	3	0.003	73
	5% V7, P	5% V7, F										70	4	0.001	-33
	5% BV	Sinusoidal	Mixed	69	-1	0.009	126	74	-3	0.002	138	70	-15	0.003	77
	5% BV	5% V3, P		70	0	0.010	135	73	-5	0.002	-129	87	-17	0.003	180
	5% BV	5% V3, F		63	-9	0.026	98	79	-8	0.005	-17	107	-11	0.006	-134
	5% BV	5% V5, P		69	0	0.009	135	71	-3	0.004	-173	79	-17	0.002	137
	5% BV	5% V5, F		69	0	0.008	132	66	-2	0.008	-170	79	-5	0.003	-49
	5% BV	5% V7, P		68	1	0.006	127	72	-5	0.003	-134	73	3	0.006	-34
	5% BV	5% V7, F		69	0	0.008	129	72	-7	0.003	-104	66	5	0.009	-22

APPENDIX B – COMPLETE SET OF TEST VOLTAGE AND CURRENT SPECTRA (SINE ANGLES)

		Personal Computer				Compact Fluorescent Lamp			
Waveform	Harmonic	V_mag	V_ang	I_mag	I_ang	V_mag	V_ang	I_mag	I_ang
Sinusoidal	1	169.4054	0	0.41979	8.0166	169.6045	0	0.77128	29.4777
	3	0.082316	324.9396	0.39328	179.1989	0.1147	98.8969	0.61168	262.8123
	5	0.10644	302.4084	0.34263	357.8375	0.22764	137.2581	0.39262	149.6234
	7	0.037248	7.3566	0.27599	176.3659	0.18778	39.1578	0.19128	54.2804
5% BV	1	169.2579	0	0.42474	355.722	169.4663	0	0.73323	25.6274
	3	7.0941	15.8793	0.38958	144.7281	6.9675	14.8605	0.40118	263.3486
	5	4.0224	203.8753	0.30902	300.5908	4.3459	203.6223	0.25309	199.7883
	7	1.6673	36.4914	0.20852	96.078	1.8663	42.1058	0.32021	105.167
5% V3, P	1	169.1152	0	0.40663	8.2455	169.2941	0	0.77185	23.796
	3	8.6448	179.8258	0.37573	180.6184	8.4605	179.1212	0.64055	249.9575
	5	0.086522	206.0563	0.34642	359.9783	0.22611	357.9269	0.45159	123.2487
	7	0.0817	97.6711	0.28792	179.8189	0.10756	225.8221	0.28468	8.1075
5% V3, F	1	169.1835	0	0.43658	8.5277	169.4769	0	0.77611	33.5365
	3	8.4933	0.1303	0.39273	179.3574	8.7821	358.4486	0.55206	276.991
	5	0.068406	113.1482	0.31301	1.0661	0.047696	266.5747	0.31595	180.7581
	7	0.47161	106.2825	0.23595	180.8933	0.22286	70.5903	0.2285	109.559
5% V5, P	1	169.3775	0	0.40859	8.8339	169.7771	0	0.77712	24.1431
	3	0.019869	273.9142	0.38615	179.6932	0.44879	246.524	0.65868	245.3649
	5	8.4756	359.7615	0.3591	359.9429	8.6643	358.1387	0.50192	110.6861
	7	0.071534	341.7655	0.31986	175.5295	0.069719	243.9613	0.30208	341.3536
5% V5, F	1	169.1771	0	0.42796	10.3905	169.7971	0	0.74561	29.3244
	3	0.058323	68.5087	0.34587	186.213	0.39323	128.6386	0.49901	272.6809
	5	8.4215	180.9889	0.22402	9.8844	8.6421	179.0411	0.36721	185.3987
	7	0.027093	247.5858	0.10391	205.6741	0.27525	76.1531	0.39765	88.7909
5% V7, P	1	169.5116	0	0.40877	6.6732	169.991	0	0.76367	23.2585
	3	0.046094	206.896	0.39583	178.3843	0.17812	267.1662	0.6129	240.5501
	5	0.062853	289.6341	0.37318	356.5991	0.12034	330.0205	0.392	98.3112
	7	8.3402	179.8069	0.3401	178.5288	9.2006	178.5973	0.17197	303.3928
5% V7, F	1	169.1142	0	0.4196	7.9116	169.7186	0	0.75921	28.0067
	3	0.053046	183.3009	0.27522	184.1419	0.040546	299.0651	0.52863	265.6998
	5	0.090147	291.193	0.089002	25.4378	0.062583	203.3533	0.41689	173.4184
	7	8.2431	0.2026	0.12454	341.6678	8.5779	0.1073	0.50789	66.3512

		Window Air Conditioner				Incandescent Lamp			
Waveform	Harmonic	V_mag	V_ang	I_mag	I_ang	V_mag	V_ang	I_mag	I_ang
Sinusoidal	1	169.6722	0	6.3764	334.489	169.6824	0	2.4614	1.0375
	3	0.20861	209.571	0.9438	109.2724	0.046319	179.4124	0.0088972	302.4267
	5	0.086088	293.0641	0.41329	214.24	0.10738	120.8424	0.00043016	15.7254
	7	0.14496	200.4917	0.027247	311.1647	0.051779	93.6105	0.0027701	248.3835
5% BV	1	169.6947	0	6.3906	334.202	169.6144	0	2.4609	1.0631
	3	7.3273	16.063	0.94973	61.1455	6.9116	17.3028	0.10402	13.0189
	5	4.6438	205.2034	0.73394	150.7884	4.2547	202.8661	0.056794	207.2836
	7	1.7658	22.0533	0.047764	283.9507	1.809	33.0242	0.022769	44.506
5% V3, P	1	169.5923	0	6.4861	335.1594	169.8896	0	2.4609	0.2445
	3	8.5057	181.0831	1.3936	126.5075	8.624	179.5616	0.11733	183.4056
	5	0.29314	95.3607	0.61261	232.6419	0.26671	100.3677	0.0049634	87.9244
	7	0.13142	210.3269	0.1505	8.1868	0.12669	66.6654	0.0034126	25.0208
5% V3, F	1	169.7526	0	6.4463	333.6449	169.7438	0	2.455	1.0528
	3	8.5993	358.1644	0.8436	56.3688	8.3758	359.693	0.13457	357.9837
	5	0.19653	322.1227	0.11931	141.8809	0.19526	152.9996	0.0071728	162.054
	7	0.14328	277.6038	0.028329	116.1403	0.12272	144.5015	0.0055649	57.6424
5% V5, P	1	169.8567	0	6.4961	334.1001	169.7515	0	2.4622	1.0592
	3	0.34736	75.0306	1.1772	104.8379	0.10226	253.6609	0.0097922	307.3328
	5	8.6759	0.896	1.1912	286.2694	8.5039	0.0406	0.12402	3.3956
	7	0.18659	83.8169	0.18341	334.3967	0.11485	161.8958	0.0014442	274.2383
5% V5, F	1	170.058	0	6.4657	333.17685	169.7643	0	2.4616	0.5034
	3	0.15844	214.0646	0.83087	86.0295	0.11675	341.8934	0.0095763	316.6915
	5	8.5295	179.8116	1.049	136.0215	8.383	179.6191	0.11873	181.4977
	7	0.3933	331.4108	0.12249	109.7922	0.05735	7.9534	0.0024509	116.2056
5% V7, P	1	170.1656	0	6.4676	333.301	169.6119	0	2.4594	359.8394
	3	0.27543	235.6314	1.0618	94.4144	0.052665	0.8085	0.0068851	312.2701
	5	0.4418	305.9252	0.48306	208.4678	0.10662	84.4398	0.0037268	61.6054
	7	8.6848	180.2556	0.73923	104.3064	8.5576	180.3606	0.12258	175.8468
5% V7, F	1	169.3709	0	6.5	334.7739	169.7644	0	2.4621	359.574
	3	0.3328	196.6066	1.0867	104.9312	0.14989	305.3566	0.01027	307.8396
	5	0.20693	59.0818	0.27608	229.1998	0.16904	158.4856	0.0041954	110.4482
	7	8.1494	358.4911	0.70289	288.6818	8.6063	359.8583	0.12213	355.6337

APPENDIX C – RESTORING INTERVAL VARIABLE DEFINITIONS

For $\omega_1 \neq \omega_2$ **:**

$$\mathbf{A} = \omega\left[\frac{e^{-\omega_1 \cdot t}}{(\omega_2 - \omega_1)\left(\omega_1{}^2 + \omega^2\right)} + \frac{e^{-\omega_2 \cdot t}}{(\omega_1 - \omega_2)\left(\omega_2{}^2 + \omega^2\right)} + \frac{\sin(\omega \cdot t - \phi)}{\omega\sqrt{\omega^2(\omega_1 + \omega_2)^2 + \left(\omega_1 \cdot \omega_2 - \omega^2\right)^2}}\right]$$

$$\mathbf{B} = \left[\frac{\omega_1 \cdot e^{-\omega_1 \cdot t}}{(\omega_1 - \omega_2)\left(\omega_1{}^2 + \omega^2\right)} - \frac{\omega_2 \cdot e^{-\omega_2 \cdot t}}{(\omega_1 - \omega_2)\left(\omega_2{}^2 + \omega^2\right)} + \frac{\sin(\omega \cdot t + \varphi)}{\sqrt{\omega^2(\omega_1 + \omega_2)^2 + \left(\omega_1 \cdot \omega_2 - \omega^2\right)^2}}\right]$$

where

$$\phi = \mathbf{tan^{-1}}\left(\frac{\omega}{\omega_1}\right) + \mathbf{tan^{-1}}\left(\frac{\omega}{\omega_2}\right)$$

$$\varphi = \mathbf{tan^{-1}}\left(\frac{\omega_1 \cdot \omega_2 - \omega^2}{\omega(\omega_1 + \omega_2)}\right)$$

$$\omega = \mathbf{2}\pi \cdot \mathbf{f_{power}}$$

For $\omega_1 = \omega_2$ **:**

$$\mathbf{A} = \left[\frac{t}{\left(\omega_1{}^2 + \omega^2\right)} + \frac{2\omega_1}{\left(\omega_1{}^2 + \omega^2\right)^2}\right]\omega \cdot e^{-\omega_1 \cdot t} + \frac{\sin(\omega \cdot t + \xi)}{\left(\omega_1{}^2 + \omega^2\right)}$$

$$\mathbf{B} = \left[\frac{\omega^2 - \omega_1{}^2}{\left(\omega_1{}^2 + \omega^2\right)^2} - \frac{\omega_1 t}{\left(\omega_1{}^2 + \omega^2\right)}\right]e^{-\omega_1 \cdot t} + \frac{\sin(\omega \cdot t + \gamma)}{\left(\omega_1{}^2 + \omega^2\right)}$$

where

$$\xi = 2 \cdot \mathbf{tan^{-1}}\left(\frac{\omega}{\omega_1}\right)$$

$$\gamma = \mathbf{tan^{-1}}\left(\frac{\omega_1{}^2 - \omega^2}{2\omega_1\omega}\right)$$

APPENDIX D – DETERMINING SYSTEM IMPEDANCE WITH PASSIVE AGENT SYSTEM IMPEDANCE MONITORING STATION

System impedance is traditionally difficult to determine due to discrepancies between electrical one-line diagrams and the actual wiring of commercial buildings. Arc hazard is determined based on the value of system impedance and therefore accuracy is important for the safety of individuals working in close proximity with high voltage electrical equipment. The hardware and software constructed and tested at Electric Power Research Institute (EPRI) allows one to directly calculate the power-frequency impedance necessary to determine arc fault current and its associated incident energy.

There have been two main techniques used to measure the driving point impedance of the power system [26]-[29]. Both techniques require voltage and current measurements on the actual power system when either 1) a load is varied or 2) harmonic current is injected into the system with either passive or active agents. The first technique has the disadvantage that the load needs to be considerably large to produce a sufficient voltage drop between the source and load. The second technique has the disadvantage that the driving point impedance can not be directly measured due to line voltage and must be interpolated from higher-order harmonic impedances. Passive agents use existing loads to inject current harmonics into the system while active agents selectively inject controlled harmonics.

The Passive Agent System Impedance Monitoring Station (PASIMS) [23] is a hybrid combination of using passive current injection and load variation to measure power frequency impedance. PASIMS uses a passive agent load to inject harmonic current into the system whose combination of harmonics creates a significant voltage drop between source and load. PASIMS therefore uses the actual voltage drop to measure the time domain driving point impedance while the frequency domain driving point impedance is interpolated and used to verify the results and identify system resonance.

PASIMS takes advantage of a power electronic load which draws distorted current for one short interval every half cycle. The current is rich in the low-order harmonics (i.e., 3rd, 5th, and 7th) with approximately the same magnitude as the fundamental. This current causes a significant voltage drop between the source and load during the time of conduction. The Thevenin equivalent source voltage when no load is applied, the load voltage when the power electronic load is applied, corresponding load current, and the Fourier derivative of current are then used to calculate the time domain power-frequency impedance between the source and load. The magnitude of low-order harmonics also provides accurate low-order harmonic impedances which are used to interpolate the power-frequency impedance. The block diagram of the station is shown in Figure D.1. The schematic of the station is given in Appendix G.

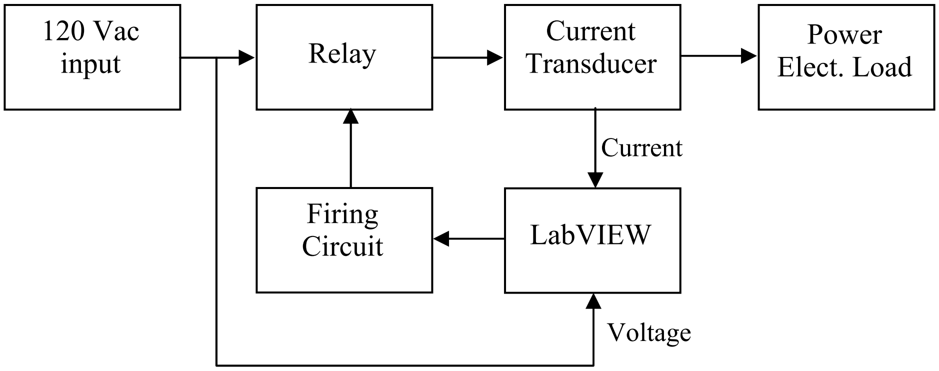


Figure D.1. Block diagram of PASIMS.

The primary advantage of PASIMS is the simplicity of design yet wealth of information provided through the load dynamics. Other advantages include:

- Single data acquisition point and online testing
- Safe, portable, and quick procedure

- Low power load (i.e., 350W on 277Vac or 100W on 120Vac)
- Passive load injects wide band of current frequencies used to determine frequency domain impedance
- Time domain driving point impedance determined from power electronic load voltage drop, current, and derivative of current
- Time domain distorted current is primarily low-order with steep slope necessary to determine accurate inductive voltage drop
- Magnitude of current pulse creates necessary voltage drop to determine accurate resistance
- Actual waveforms reconstructed using Fourier series, thus reducing noise
- FFT averages the Thevenin equivalent source and load waveforms over 60 cycles to filter momentary changes in the system and provide more accurate FFT results
- Recursive procedure shifts Thevenin equivalent open circuit voltage phase angle and solves for impedance until solution converges
- Multiple tests give average value results with small standard deviation
- Resonance and voltage error checks
    - The presence of capacitor banks cause resonance seen in the impedance scan which can effect results
    - Error is determined from difference in Thevenin source and load voltage during power electronic load non-conduction interval

D.1 Application

The application of the station includes:

- Source impedance testing
    - Line-to-line
    - Line-to-neutral
    - Arc flash hazard
    - Incident energy
- Transformer series impedance testing
- Component series impedance
- Identification of resonance and capacitor banks

The station, designed for single-phase, can easily be implemented to three-phase allowing the impedance of Z_{ab}, Z_{bc}, and Z_{ca} to be determined. Using the two sets (real and imaginary) of three equations and three unknowns,

$$R_{ab} + j\omega L_{ab} = (R_a + R_b) + j\omega(L_a + L_b), \tag{D-1}$$

$$R_{bc} + j\omega L_{bc} = (R_b + R_c) + j\omega(L_b + L_c), \tag{D-2}$$

$$R_{ca} + j\omega L_{ca} = (R_c + R_a) + j\omega(L_c + L_a), \tag{D-3}$$

one can solve for the individual conductor impedances. Knowing these, one can then solve the impedance of Z_{ln} and determine the neutral conductor impedance:

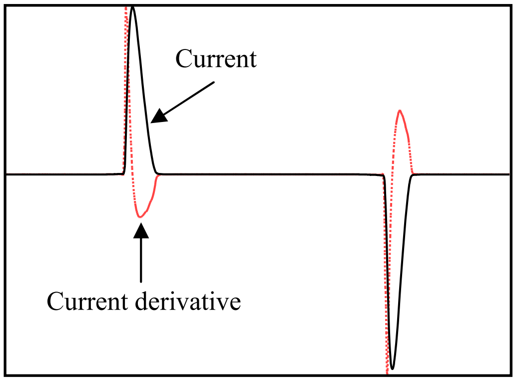
$$R_{an} + j\omega L_{an} = (R_a + R_n) + j\omega(L_a + L_n). \tag{D-4}$$

For industrial applications, the phase-to-phase mutual impedance is negligible and can therefore be neglected. The impedance measured will approximately be the positive sequence impedance.

D.2 Theory of Operation

D.2.1 Frequency domain solution

The characteristics of the power electronic load make it a useful tool to determine frequency domain harmonic system impedance. Any load, specifically those whose current waveform is rich with harmonics besides the fundamental, can inject harmonics into the power system. These loads are passive agents in which under normal operation, they inject harmonic current into the system. A typical power electronic load current has the waveshape seen in Figure D.2. The harmonic current magnitudes can be seen to the right of the waveform normalized to the fundamental.



Harmonic	% Magnitude
1	100
3	98
5	94
7	89
9	82
11	75
13	66
15	58
17	49
19	40
21	32
23	25
25	18

Figure D.2. Power electronic load current for one power frequency cycle with harmonic magnitudes normalized to the fundamental.

The dominant frequencies include the fundamental through the 7th harmonic. The harmonics not listed, odd and even, are each less than 15%. Each current frequency introduces a corresponding harmonic voltage due to the harmonic impedance. One can therefore solve for the harmonic impedance by using the difference in harmonic voltage during and prior to when the passive load was placed online and the harmonic current by

$$Z_h = \frac{\Delta V_h}{I_h} . \tag{D-5}$$

Using a Line Impedance Stabilization Network (LISN) in accordance to standard MIL-STD-461E, the impedance of the source providing input power to PASIMS is controlled regardless of the power system. The LISN then controls the impedance seen by PASIMS in the range of 10kHz-10MHz. The magnitude of current injected from PASIMS at these frequencies is low; however, impedances could still be determined. When using the LISN, the trend of calculated harmonic impedances for 10kHz-48kHz match within the given tolerance as seen in Figure D.3. The highest harmonic possibly measured with PASIMS is at 48kHz, so no higher measurements could be made.

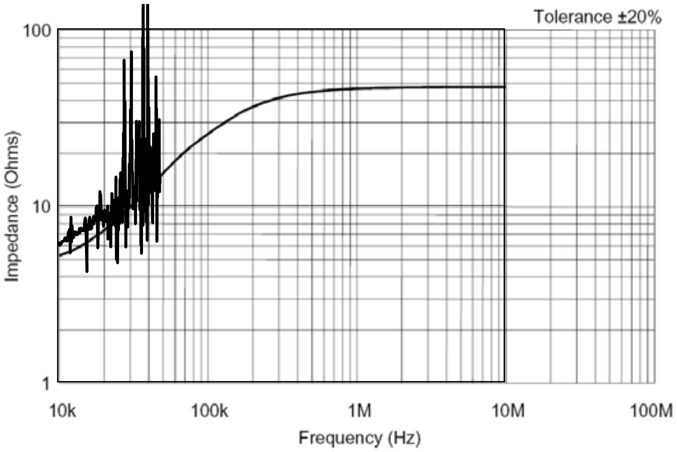


Figure D.3. LISN harmonic impedance curve (smooth line) with superimposed PASIMS solution.

The harmonic solution also works well for low-order harmonics; however, the line voltage causes errors in the solution at the power frequency. The harmonic system impedance at a 120Vac lab outlet is plotted in Figure D.4 for odd harmonics through the 59th multiple. It can be seen that the power frequency solution for inductance is higher than the trend of harmonic inductance would predict. The solution at the power frequency can not be directly determined with this approach, and therefore must be interpolated from non-fundamental harmonics.

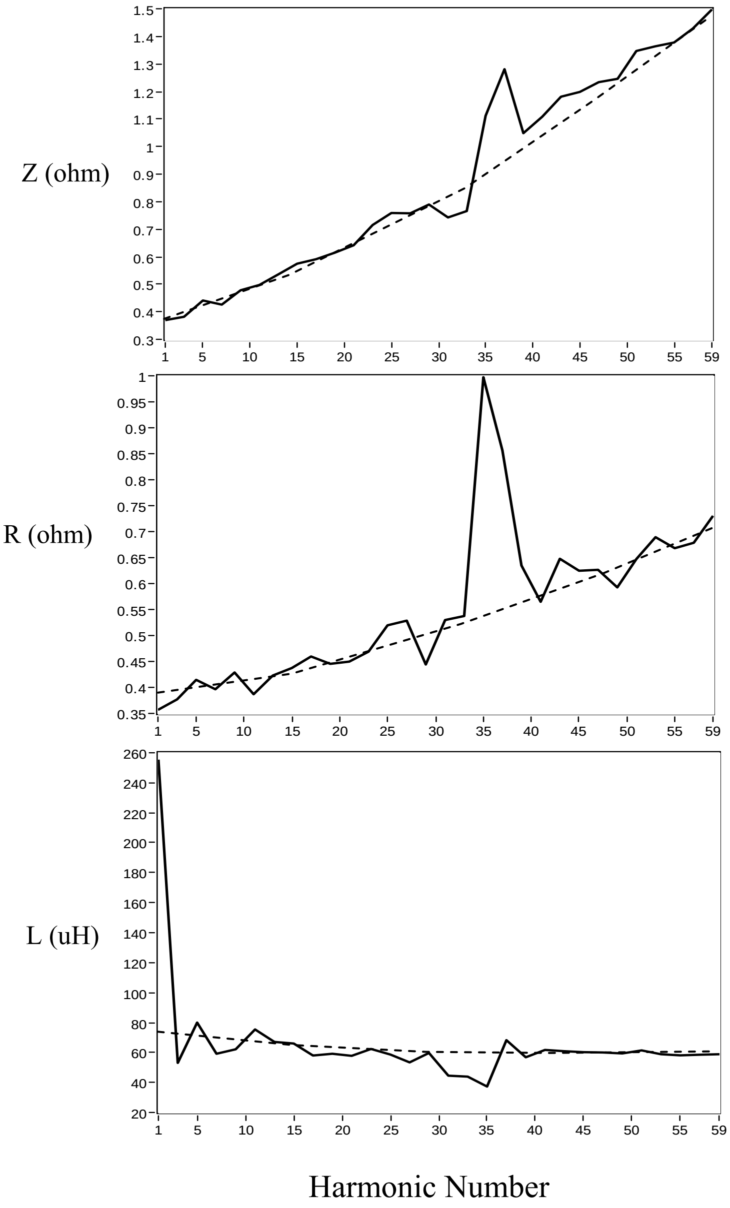


Figure D.4. Actual 120Vac frequency domain impedance scans with dashed trend-line.

If there were a capacitor bank on the system near the point of measurement, then the frequency domain impedance scan would show an increase in impedance near the resonant frequency which is closely identified by $f = \frac{1}{2\pi\sqrt{LC}}$. The resonant frequency, however, will be skewed because the system resistance is in series with the system inductance, and these are in parallel with the capacitor bank and its resistance.

The harmonic impedance is the parallel combination of system and capacitor bank impedance derived as

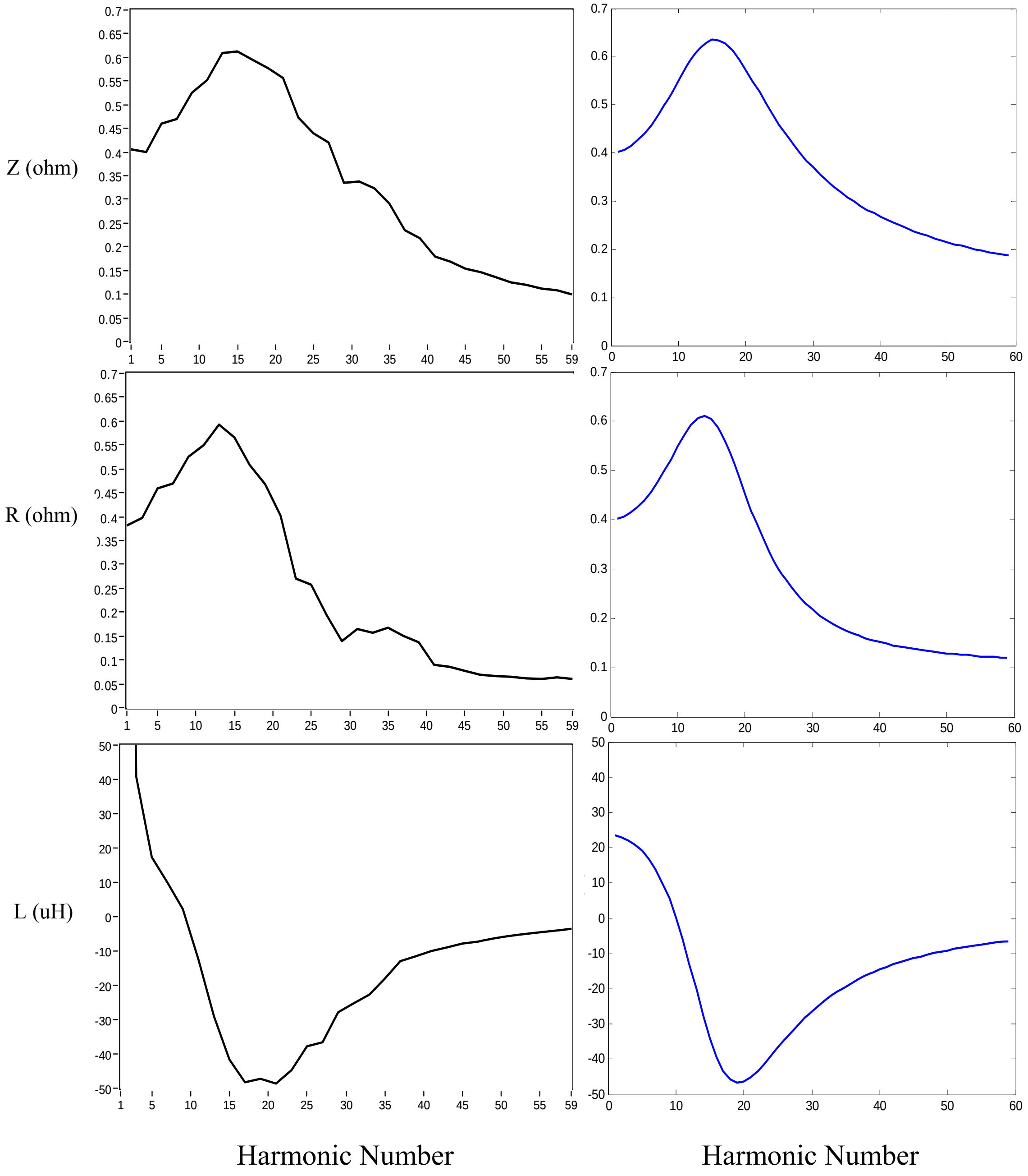
$$Z_h = \frac{R_s R_c + {}^{L_s}\!/_{C} + {}^{R_s}\!/_{j\omega C} + j\omega L_s R_c}{R_s + R_c + j\omega L_s + {}^{1}\!/_{j\omega C}} . \tag{D-6}$$

At the resonant frequency, the parallel impedance of the system and capacitor causes the derived impedance to increase due to the cancellation of the harmonic inductive and capacitive terms in the denominator. The resultant resonant frequency impedance can be closely approximated disregarding the capacitor resistance by

$$Z_h = \frac{L_s}{R_s C} - j\frac{1}{\omega C} . \tag{D-7}$$

The real part is therefore influenced by the inductive and capacitive elements while the imaginary part is capacitive.

Capacitor banks have a significant impact on the harmonic impedance when the resonance is near the fundamental. On the same system as in the previous example where R_s = 0.4ohms and L_s = 74uH, a 315uF (≈ 2kVAr) capacitor bank will cause resonance near the 17th harmonic. This resonance can be seen in the impedance scan of Figure D.5. To the right of these, the harmonic impedance is analytical solved for the system parameters and an approximate capacitor bank resistance of 0.1ohm. In the presence of this capacitor bank, interpolating the driving point inductance gives under-estimated results while the interpolated resistance remains accurate.



(a) (b)

Figure D.5. (a) Actual and (b) analytical frequency domain solutions for system impedance in the presence of a 315uF capacitor bank.

D.2.2 Time domain solution

The actual time domain response of the system due to the power electronic load is a dip in voltage only at the peak of the voltage waveform. This is due to the design of the power electronic load to have approximately 5% DC voltage ripple. For PASIMS, a relatively small load (100W on rectified 120Vac or 350W on rectified 277Vac) causes a significant voltage dip as seen in Figure D.6.

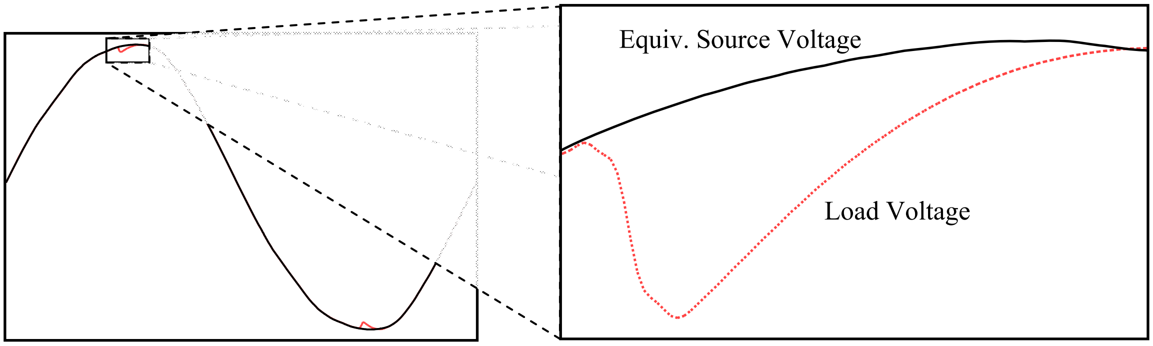


Figure D.6. Voltage dip caused during conduction interval of power electronic load.

The initial procedure to measure system impedance was to take the actual load voltage and fit it with the power electronic load components in Figure D.7, drawn without the diode bridge during the conduction interval. From this, one can determine the associated load current. Working from the load back to the system, one would then solve for the best fit impedance to match the Thevevin equivalent source voltage.

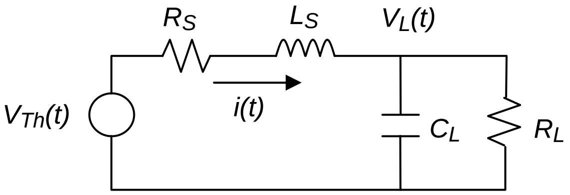


Figure D.7. System and power electronic load schematic during conduction interval

Another approach is to use the power electronic load dynamic response equation to solve for system impedance. The power electronic load has a DC capacitor to store charge for the part of the cycle in which the load is effectively disconnected from the system. This occurs when the AC voltage is less than the DC capacitor voltage. The DC capacitor receives the majority of power during the conduction period to restore what was displaced during non-conduction. The dynamics of this circuit can be described with the second-order linear differential equation

$$V_{Th}(t) = L_S C_L \frac{d^2 V_L(t)}{dt^2} + \left(R_S C_L + \frac{L_S}{R_L} \right) \frac{dV_L(t)}{dt} + \left(\frac{R_S}{R_L} + 1 \right) V_L(t) \qquad \text{(D-8)}$$

which can be reduced because $R_S C_L >> \frac{L_S}{R_L}$ and $\frac{R_S}{R_L} << 1$, yielding

$$V_{Th}(t) = L_S C_L \frac{d^2 V_L(t)}{dt^2} + R_S C_L \frac{dV_L(t)}{dt} + V_L(t). \qquad \text{(D-9)}$$

This equation can be used to solve in the time domain the system impedance using only voltage data and Least Squares over the conduction interval; however, the actual voltage waveforms must have a significantly small amount of noise to make it possible to attain the second derivative of load voltage either numerically or using the FFT. Reducing noise with sampling capacitors or filters is problematic due to the slew of the filtered waveform. Sharp signals are necessary to solve using Least Squares. Noise has been found to be problematic and leads to a more refined approach.

The power electronic load conduction current is more attractive over a 60Hz current because it has a high magnitude with a steep slope over a short duration providing a significant derivative with minimal influence from noise. Using the actual load conduction current and actual change in voltage, one can bypass the load dynamics and directly solve in the time domain for the system impedance using Least Squares over the conduction interval with the following equation:

$$V_{Th}(t) = R_S \cdot i(t) + L_S \frac{di(t)}{dt} + V_L(t). \qquad \text{(D-10)}$$

The initial solution assumes the Thevenin equivalent source and load voltage are in-phase. The solution is then used to solve for a new Thevenin equivalent source voltage phase angle. After shifting the source voltage, the impedance is resolved and the process is repeated until the solution converges.

D.2.3 Hybrid combination of results

Using both procedures provide a way to check the system impedance results. Under most system configurations the results will be similar, however, in the case of resonance, the results can vary. In resonant conditions, which can be seen in the frequency domain impedance scan, the interpolated frequency domain resistance remains closer to the actual system resistance while the time domain inductance is remains closer to the actual system inductance. Using both techniques in resonant conditions is important. In other conditions, the time domain solution provides more accurate driving point impedance results because no interpolation is necessary.

D.2.4 Error analysis

Error in the power frequency time domain solution can exist if nearby feeder load is changing. The more time elapsed between Thevenin equivalent source and load measurements can increase the chance of large loads coming on-line or going off-line. These changes in load are easily identified by the difference between load and source voltage waveforms during the non-conduction interval of PASIMS test load. The time domain difference should be zero between test load conduction intervals if the system remains constant; however, if the equivalent source voltage is greater than the load voltage as in Figure D.8, the system impedance will be over-estimated because it looks as if there was a greater voltage drop. If the equivalent source voltage is less than the load voltage, the system impedance will be under-estimated. By Ohm's law, system resistance is proportional to voltage drop such that $V_{drop} + \Delta V = I \cdot (R + \Delta R)$ and $\Delta R = \frac{\Delta V}{I}$.

ΔR varies with ΔV which can cause the solution to be over- or under-estimated.

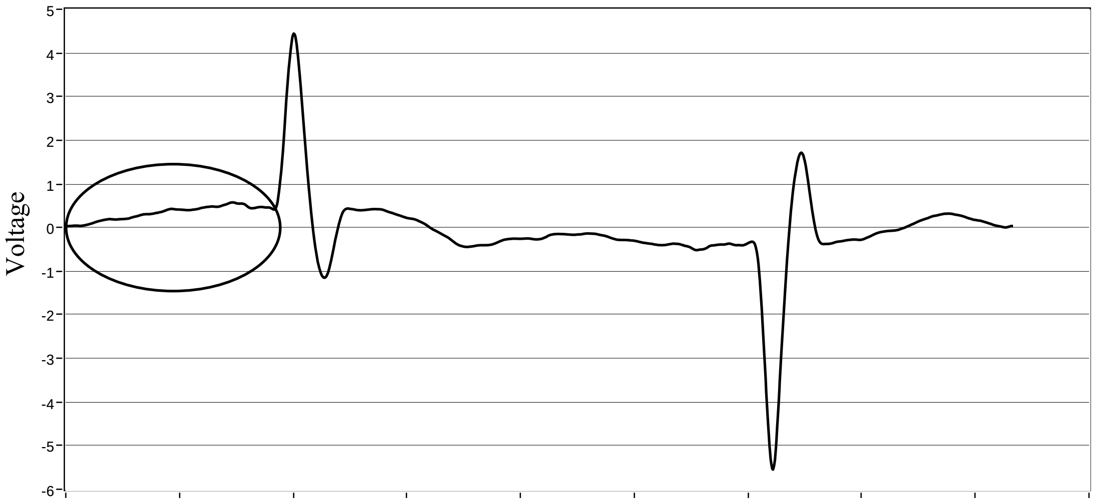


Figure D.8. Voltage drop for one power frequency cycle. Circled region for first quarter cycle shows the solution will be over-estimated.

Typical noise will cause the change in voltage to oscillate by a small amount around zero during the non-conduction interval, but this has a negligible impact on the results. If the absolute value of 60Hz change in non-conduction voltage is greater than a selected percent of system voltage, the station will report that the impedance error is significant. 0.064% has been found to be an appropriate limit. In resonant conditions the error will always appear to be large and therefore must be disregarded.

D.3 Test Results

D.3.1 120Vac insertion

Several series insertion devices were used to analyze the time domain solution for series impedance. The six insertion devices include a fuse, 0.1ohm resistor, 0.05ohm resistor, 0.2ohm resistor, 100uH inductor with DCR < 0.03ohm, and 0.1ohm resistor in series with 100uH inductor. Each insertion device was compared to the solution from a direct connection to extract the resistance of the insertion device. Five tests were used in each situation, and the averages were taken and plotted in Figure D.9. In each situation, the new system resistance changed by approximately the rating of the insertion device. PASIMS could also determine that components such as the insertion fuse and terminal connections increased system resistance. The standard deviation of results for each insertion device is approximately 0.015ohms and 1uH. The error in individual test results can be identified by the difference in voltage during and prior to the application of test load while in non-conduction. The difference should be zero between conduction intervals if the system remains constant, however, if large loads come on-line or drop from the system, the time domain solution for system impedance will incur error. Using the voltage error check, solutions with error can be identified and the impedance error can be further minimized.

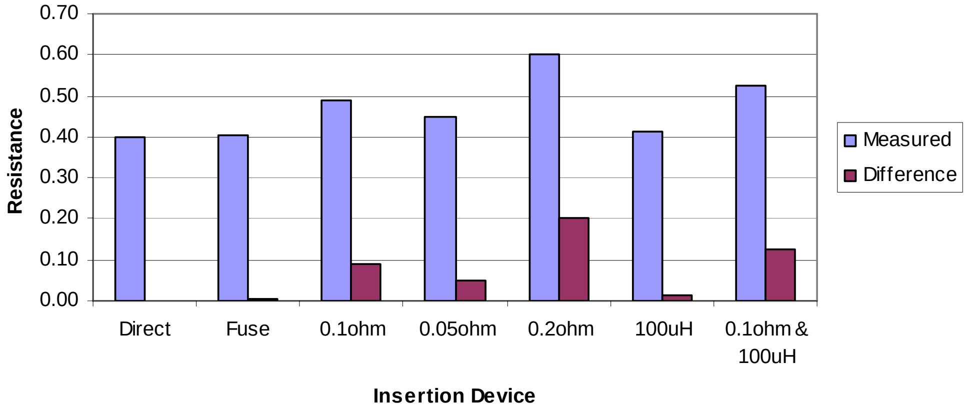


Figure D.9. 120Vac time domain system resistance for insertion devices.

D.3.2 120Vac parallel load

It is possible that when testing system impedance there will be other loads online that will obscure the test results. In most cases, the impedance of these other loads will be at least 20 times larger than the system impedance and therefore not affect the solution. However, parallel loads such as other power electronics or capacitor banks can obscure the results.

The worst case is when the a parallel load is an unloaded capacitor bank located near the measurement point; however, the transient inrush from the bank to the station decays fast enough that the Least Squares solution remains similar to that solved if the bank did not exist. If there is an inductance between the bank and the station, the transient will take longer to decay, but the solution will only be slightly skewed due to the location of the bank.

Similar to PASIMS, other power electronic loads take a significant amount of power at the peak of the voltage waveform and can alter the results of the station. In Figure D.10, the time domain results are given for several different parallel loads including various capacitor banks, a personal computer (40W), personal computer and monitor (120W), and a large incandescent lamp bank (400W). In each situation, the system impedance changes due to the influence of the parallel load. The greatest consequence is the increase in system resistance for the 315uF capacitor bank and the decrease in system resistance and inductance for the large power electronic load.

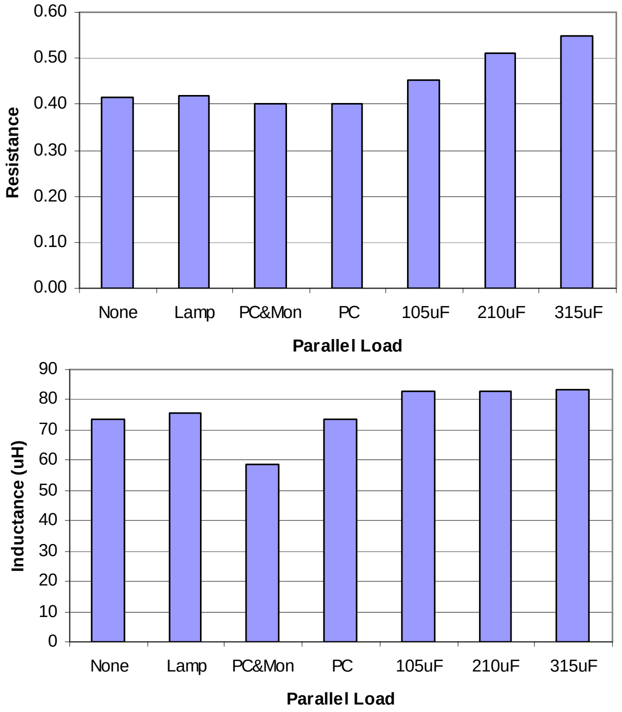


Figure D.10. 120Vac time domain system resistance and inductance with parallel loads.

Large capacitor banks, identified by resonance near the fundamental, have a significant impact on the time domain system impedance. A purpose of a capacitor bank is for voltage support, increasing the voltage at the receiving end of the line. Therefore, an unloaded capacitor bank will cause the measured Thevenin equivalent open circuit source voltage to appear greater than the actual system source voltage. When the PASIMS load is placed on-line, the capacitor bank becomes loaded and the voltage difference will appear to be caused by a larger resistive voltage drop. Therefore, resistance is over-estimated while inductance remains closer to the actual value.

The entire conduction interval does not provide the best solution for the time domain driving point impedance when capacitor banks or a large amount of power electronics are located nearby. In these situations where there is a capacitive inrush to the load or the Thevenin voltage is flattened, the best solution is found using the second half of the conduction interval.

D.3.3 120Vac scan rate and waveform reconstruction

It was found that the sampling rate has an effect on the time domain solution. As shown in Table 6.1 for five test averages, lower sampling rates result in higher R and lower L while lower harmonics results in lower R and higher L. 100ksamp/sec over three cycles is necessary for good FFT results to reconstruct the actual waveform. Lower sampling would be sufficient if more cycles were to be averaged with the FFT. The typical power electronic load current can be reconstructed with as low as 20 harmonics; however, higher harmonics are necessary for good inductance results. Higher harmonics are also necessary when capacitive loads are located nearby which cause an inrush transient at the onset of the conduction interval. In this case, the harmonic magnitudes are altered from those in Figure D.2, and as many as 300 harmonics are necessary for waveform reconstruction.

Table D.1. Sampling Rate vs. Harmonics Used in Waveform Reconstruction.

	Harmonics Used for Waveform Reconstruction					
	100		50		20	
Sampling Rate	R	L (uH)	R	L (uH)	R	L (uH)
100ksamp/sec	0.40	64	0.40	65	0.40	68
50ksamp/sec	0.41	61	0.41	63	0.40	66
20ksamp/sec	0.43	60	0.42	62	0.42	65

D.3.4 277Vac insertion

With simple modification to maintain 5% DC voltage ripple, PASIMS was then tested at 277Vac. Again with the same insertion devices as in the 120Vac test, one can determined the insertion device impedance. In Figure D.11, the resistance and inductance are solved in the time domain for different insertion devices and plotted for each of the three phases located at Disconnect 3a in the EPRI-PDM lab. The plotted results are the average of five tests with an approximate standard deviation of 0.01ohms and 1uH. In each situation, the increased impedance is approximately the insertion components rated value.

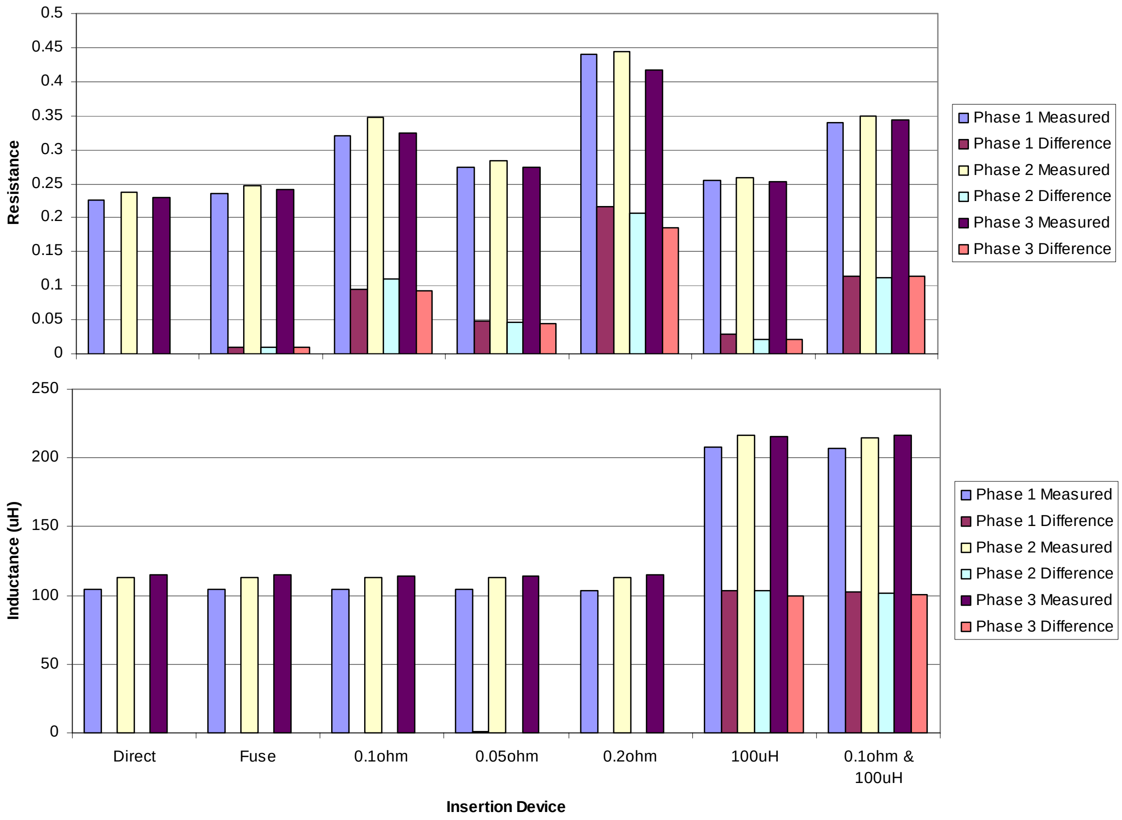
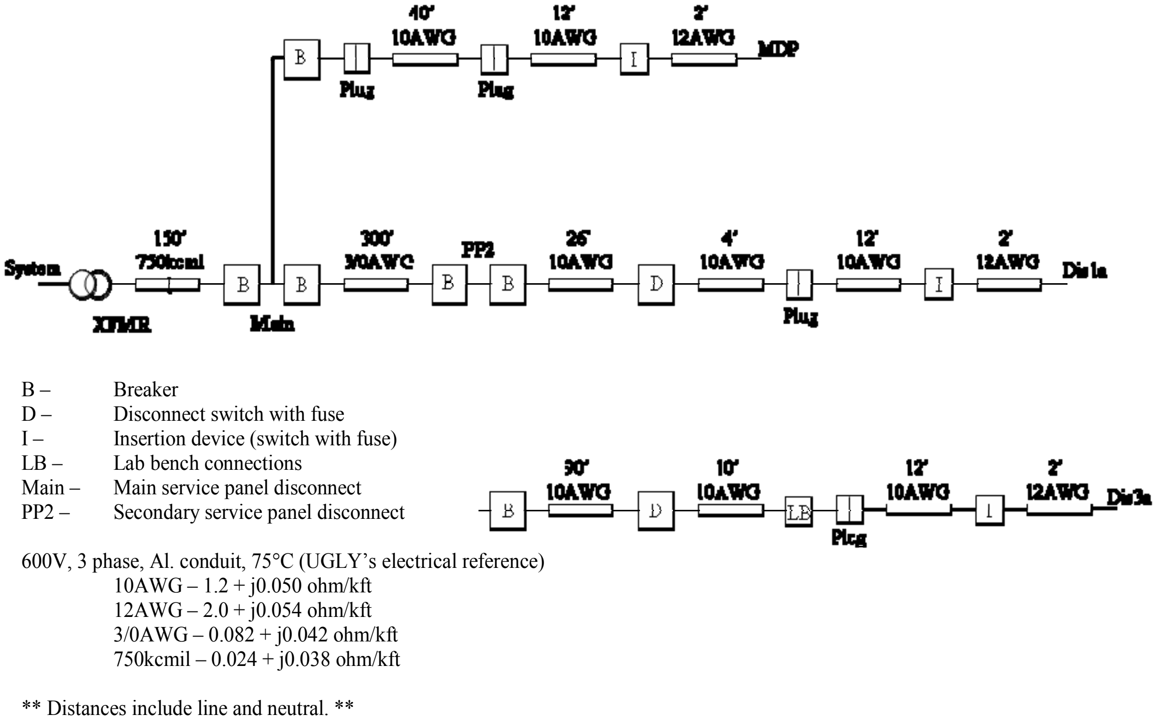


Figure D.11. 277Vac time domain system resistance and inductance for insertion devices.

D.3.5 277Vac location variation

The next test was to solve for the system impedance on a known circuit in the EPRI-PDM lab. The building circuit one-line diagram can be seen in Figure D.12 along with miscellaneous connections, breakers, and other elements that cause additional impedance. There were three test locations on the circuit fed from the building transformer: MDP (near main disconnect panel), Dis1a (near sub-panel PP2), and Dis3a (off sub-panel PP2). At each test location, the difference in phase impedance is due to circuit elements such as cables, connections, and switches between locations. Cable impedance was approximated using values from UGLY's Electrical Reference, and the remaining connections were taken into consideration having a small (≈ 3 milliohms) but important series resistance. The remaining line impedance is up to the high side of the Y-Y 7620/480V, 300KVA, 3.17%Z building transformer. Using these ratings and X/R = 1.5, the transformer resistance would be approximately 0.014 ohms, and the inductance would be approximately 54uH.



B – Breaker
D – Disconnect switch with fuse
I – Insertion device (switch with fuse)
LB – Lab bench connections
Main – Main service panel disconnect
PP2 – Secondary service panel disconnect

600V, 3 phase, Al. conduit, 75°C (UGLY's electrical reference)
10AWG – 1.2 + j0.050 ohm/kft
12AWG – 2.0 + j0.054 ohm/kft
3/0AWG – 0.082 + j0.042 ohm/kft
750kcmil – 0.024 + j0.038 ohm/kft

** Distances include line and neutral. **

Figure D.12. 480Vac building one-line diagram.

The time domain solution averaged over five tests for each phase and location has a standard deviation of approximately 0.01ohms and 1uH. The results for the three test locations are given in the first three sets of data in Figure D.13. The one-line diagram impedance from Dis3a and Dis1a to PP2 can be used to determine the system impedance at the sub-panel breaker PP2. The impedance at this location is closely identical from Dis1a and Dis3a. These results are shown in the 4th and 5th sets of data in Figure D.13. From PP2, the impedance is further solved back to the main breaker. The system impedance at the main breaker from MDP is similar to the impedance from PP2. These results are shown in the 6th, 7th, and 8th sets of data in Figure D.13. Furthermore, each location can be used to work back to the building transformer impedance. These results are given in the last three sets of data in Figure D.13 and are similar to the building transformer impedance rating. Variations in results per phase are most easily identified as differences in cable and contact impedances along with how well terminals are connected together.

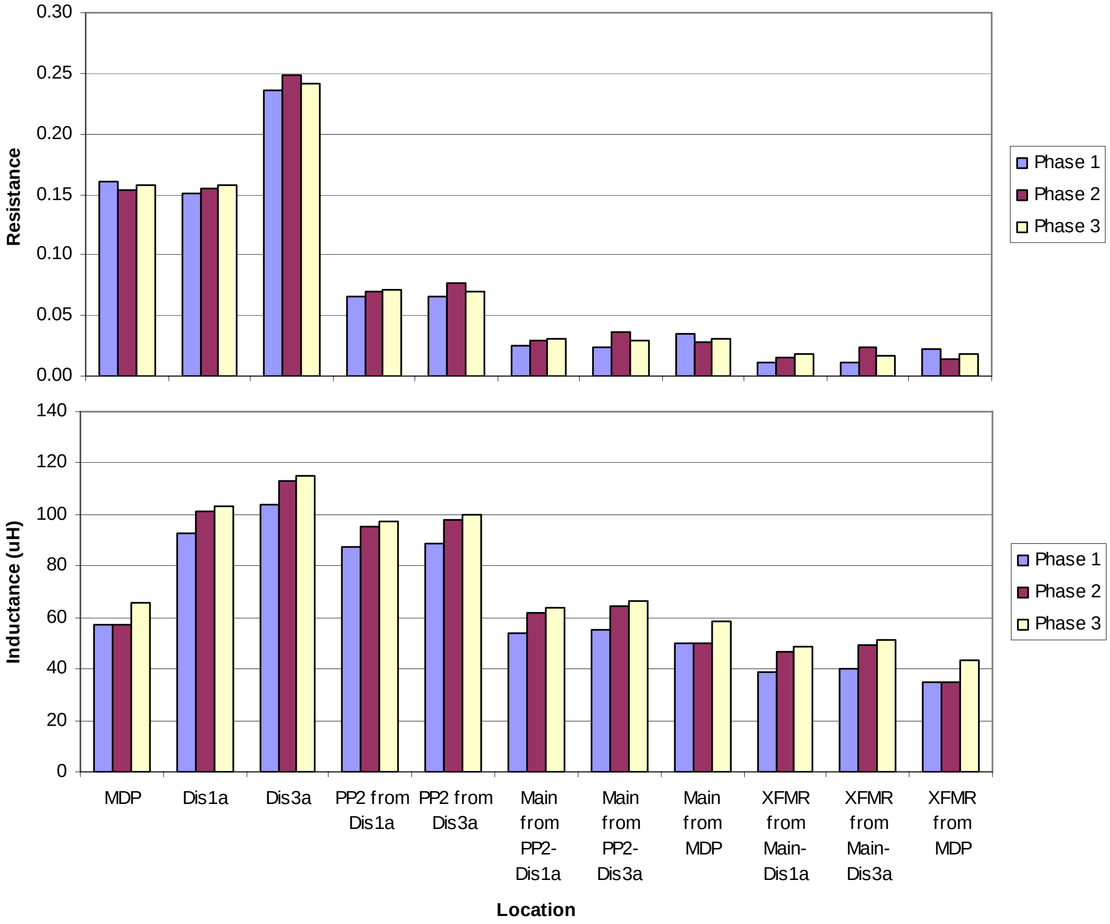


Figure D.13. 277Vac time domain impedance for three test locations and solving back to points of common coupling.

D.4 Summary

PASIMS incorporates two techniques (time domain and frequency domain) to solve for system impedance and takes advantage of the good qualities in each. The station has been validated with insertion devices, parallel loads, at various locations on a known feeder, and with a LISN. The primary advantage of PASIMS is the simplicity of design yet wealth of information provided through the load dynamics.

D.5 Station Operating Procedure

1. Start software
2. Run initialization test
    - Compare actual load current to reconstructed current waveform
        - 100 harmonics is sufficient for typical power electronic current waveforms similar to Figure D.2, however, in the presence of capacitor banks or flattened building voltage which alter the harmonic composition, as many as 300 harmonics can be necessary
        - If actual and reconstructed current waveforms look different, increase the number of harmonics used for waveform reconstruction
    - Choose conduction cycle points to be solved with Least Squares estimation
        - Using the fundamental current phase angle this is determined automatically to begin near the onset of the current conduction interval and continues until the current goes back to zero
        - The entire load conduction interval provides best results when no resonance is visible in the harmonic impedance scan
        - If there is resonance and a transient in-rush of current from the capacitor bank to the power electronic load each half cycle, choose the second half of the conduction cycle as the points to be solved with least squares
    - If changes were made, restart software and continue to (3)
3. Thevenin equivalent source (open circuit) measurements are made for 2.5 seconds for voltage and current at 100ksamp/sec with a 16 bit data acquisition card while the load is ‘off’
4. A solid state relay controlled by a timer provides isolation and turns the power electronic load ‘on’ for 2.5 seconds while load measurements continue to be made
5. (3) and (4) are repeated for desired number of tests. Three tests are shown in Figure D.14.

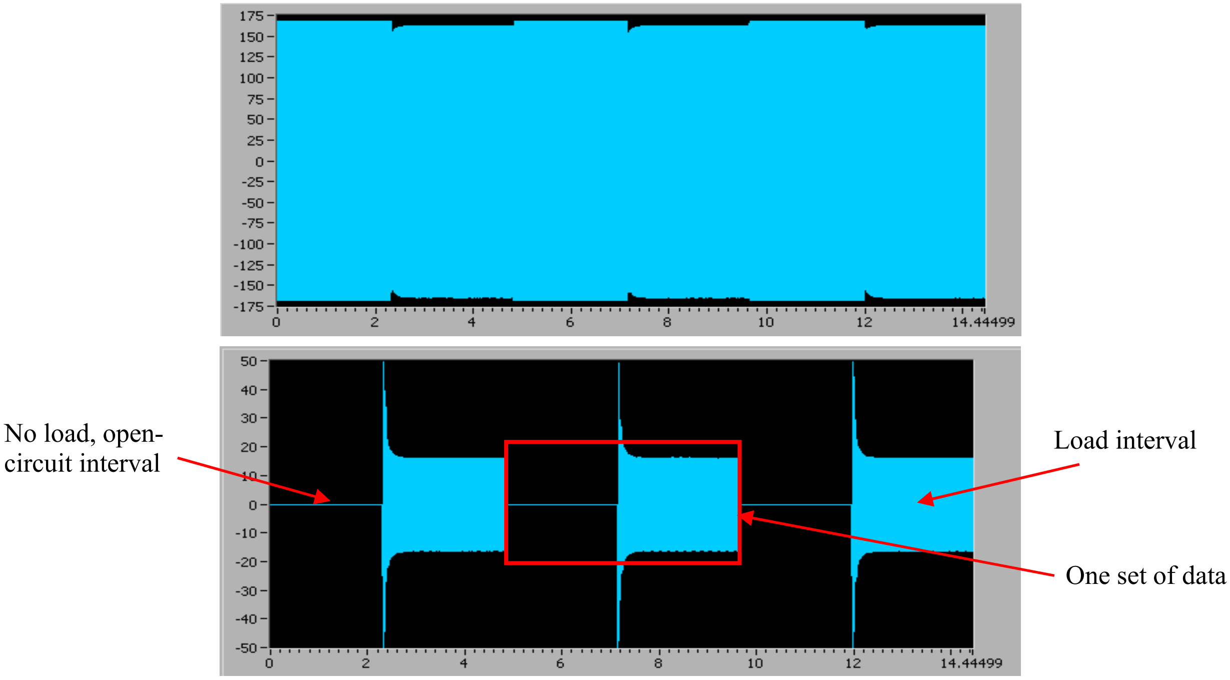


Figure D.14. Voltage (top) and current (bottom) waveform for three consecutive impedance tests.

6. FFT is performed over 60 cycles of Thevenin source measurements
7. FFT is performed over 60 cycles of steady state load waveform measurements
    - This occurs no earlier than 10 cycles after load turns 'on'
    - In-rush transient to load is not desired
    - Thevenin source and load FFT's should be close together in time to minimize chance of nearby load change
8. FFT averages the cycles, thus reducing influence of noise and momentary changes in waveforms
9. Begin analyzing data
    - Reconstruct the waveforms for voltage and current
        - Create a waveform for load current derivative by differentiating the Fourier series of load current
        - One cycle reconstruction with 1667 points has been found adequate and more time efficient without effecting results
    - At this time, voltage fundamental when load is 'off' is assumed in-phase with the voltage fundamental when load is 'on'
    - Thevenin source and load waveforms are aligned in-phase
    - DC offset of current probe is determined by observing DC component of FFT while the load is 'off'
        - In open circuit, current should be zero

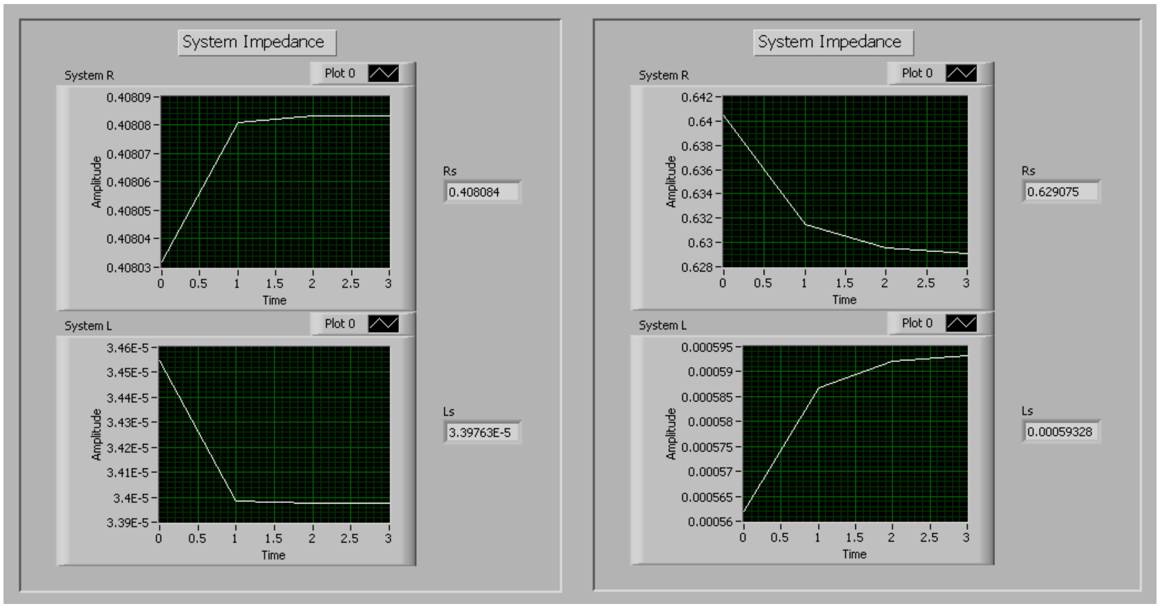
10. Solve in the time domain with Least Squares iteration n of system impedance $R^{(n)}$ and $L^{(n)}$ with the over-defined equation

$$[V_{Th}(t) - V_L(t)] = \begin{bmatrix} I_L(t) & \dfrac{dI_L(t)}{dt} \end{bmatrix} \cdot \begin{bmatrix} R^{(n)} \\ L^{(n)} \end{bmatrix}.$$

11. After the best solution is determined, a new Thevenin source voltage is solved using

$$V_{Th}(t) = \begin{bmatrix} I_L(t) & \dfrac{dI_L(t)}{dt} \end{bmatrix} \cdot \begin{bmatrix} R^{(n)} \\ L^{(n)} \end{bmatrix} + V_L(t),$$

and a new Thevenin source phase angle is calculated using the FFT. The actual Thevenin source voltage is shifted, and $R^{(n+1)}$ and $L^{(n+1)}$ are determined. This recursive approach is followed until the solution converges.
    - The number of iterations necessary for the solution to converge depends on the magnitude of the source impedance.
    - Typical convergence occurs in three to four iterations. Four iterations are shown in Figure D.15a for small system impedance and in Figure D.15b for large system impedance.



Rs 0.408084

Ls 3.39763E-5

Rs 0.629075

Ls 0.00059328

(a) (b)

Figure D.15. Convergence of resistance and inductance for (a) small system impedance and (b) large system impedance.

12. Calculate non-conduction voltage error to determine if the direct solution is under- or over-estimated
    - Change in non-conduction voltage identifies drop or increase of large nearby loads

- Fundamental change between load and Thevenin source voltage should be minimized
    - Less than 0.064% fundamental voltage change is adequate for good results

13. Solve for the harmonic impedance

$$Z_h = \frac{\Delta V_h}{I_h}$$

- Complex harmonic impedance is split into real and imaginary components to determine resistance and inductance
- Driving point impedance must be interpolated from trend of non-fundamental harmonics
- Type of interpolation depends on the system conditions such as resonance
    - 3rd harmonic closely resembles driving point impedance
- If resonance is near fundamental, use frequency domain interpolated driving point resistance and time series inductance

14. Plot results and deliver solution to user. Three solutions for system impedance are shown in Figure D.16.

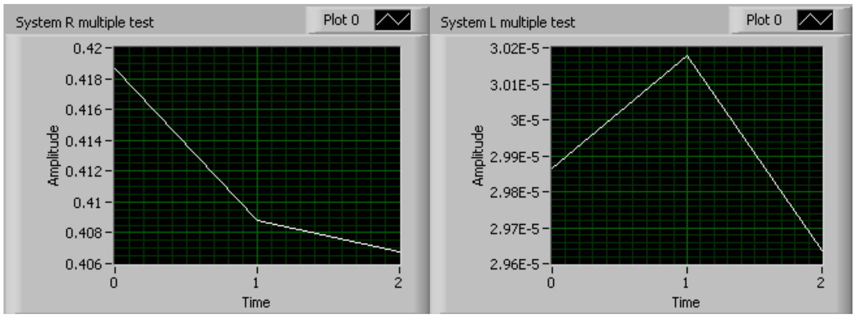
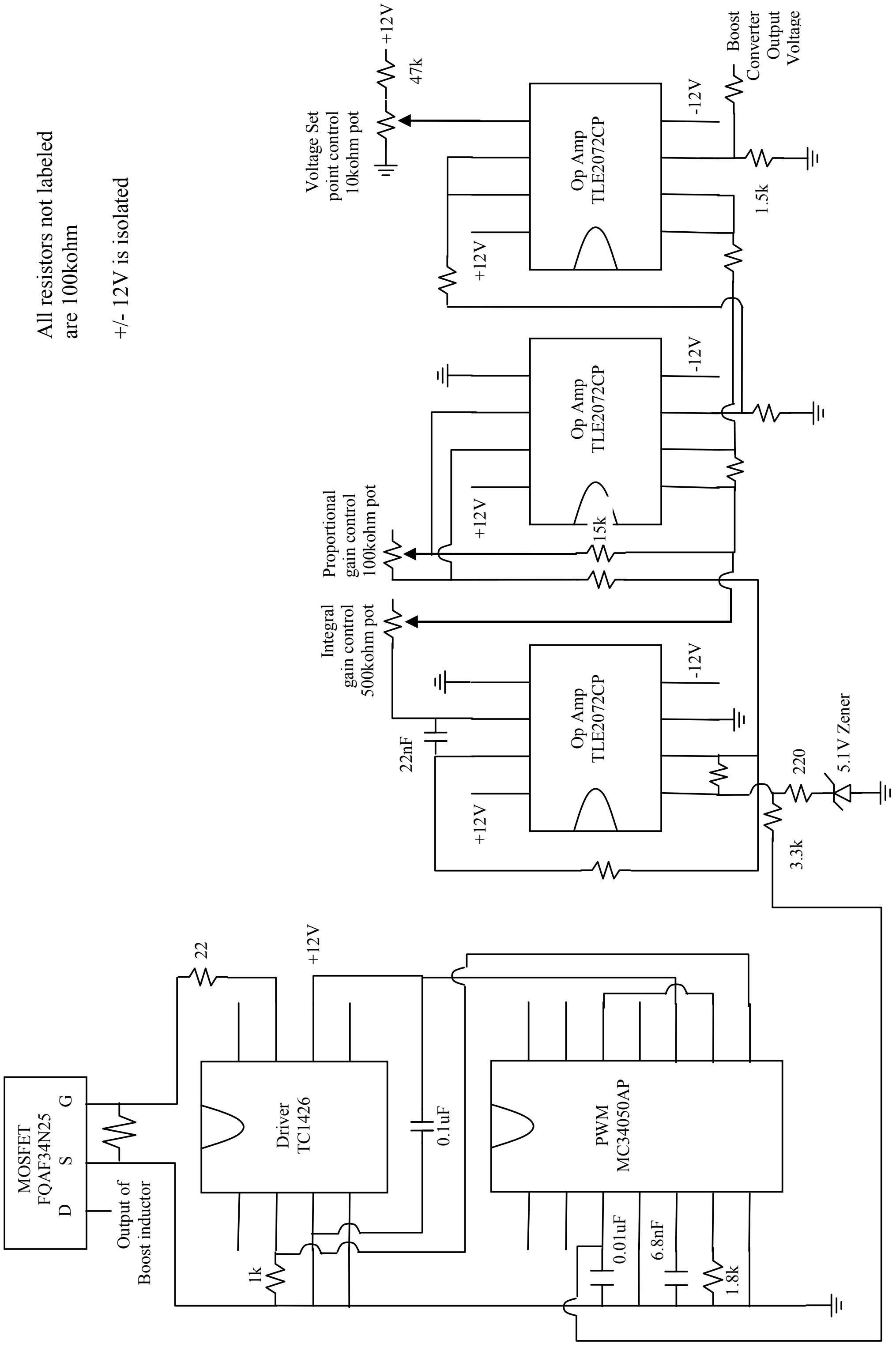


Figure D.16. Three consecutive impedance tests.

15. Software stops

APPENDIX E – PROPORTIONAL/INTEGRAL DUTY CYCLE CONTROL SCHEMATIC



APPENDIX F – UNIVERSITY OF TEXAS AT AUSTIN POWER SYSTEM DATA

All values are on generator MVA base

Generator		**7**		**8**		**9**		**Ercot**
MVA base		32		53.9		32		1000
KV		12		12		12		69
pf		0.9		0.9		0.85		0.9
PSSE Type		GENROU		GENROU		GENSAL		GENROU
T'do		3.42		6.01		6.124		6.5
T"do		0.034		0.06		0.047		0.06
T'qo		0.332		0.67				0.2
T"qo		0.056		0.098		0.09		0.05
H		2.43		1.321		1.3648		10000
D		0		0		0		0
Xd		1.819		2.328		2.1		1.8
Xq		1.747		2.268		1.9		1.75
X'd		0.3		0.364		0.217		0.6
X'q		0.574		0.586				0.8
X"d		0.209		0.202		0.155		0.12
Xl		0.065		0.16		0.099		0.15
S(1.0)		0.03		0.03		0.153		0.09
S(1.2)		0.4		0.4		0.899		0.38

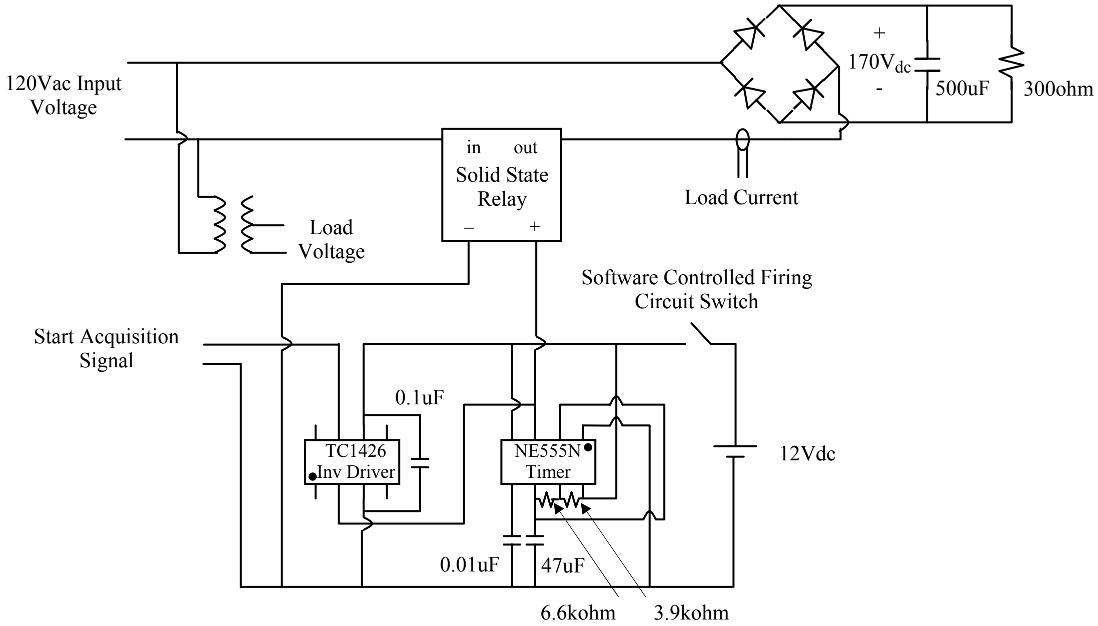
Exciter of Generator 8 modeled for all UT Generators

Exiter Type		EXST1
Tr		0
Vimax		2.4
Vimin		-2.4
Tc		0
Tb		0
Ka		250
Ta		0.02
Vrmax		6
Vrmin		-5.1
Kc		0.05
Kf		0.003
Tf		1

Load Model

		% Constant I		% Constant Z
Real Power		50%		50%
Reactive Power		25%		75%

APPENDIX G – SCHEMATIC OF PASSIVE AGENT SYSTEM IMPEDANCE MONITORING STATION



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Vita

Matthew Robert Rylander was born in Austin, Texas on September 23, 1981, the son of Margaret Susan Rylander and H. Grady Rylander III. After earning a diploma from Leander High School, Leander, Texas, in 2000, he entered the University of Texas at Austin in the College of Electrical and Computer Engineering. In 2004, he graduated with honors with a Bachelor of Science Degree in Electrical Engineering. Immediately following graduation, he enrolled in the electrical engineering graduate program at the University of Texas at Austin where he earned his Masters of Science in Engineering degree in 2006. His primary focus has been on harmonics, load modeling, and power system stability. He has constructed a Voltage Sag-Test Station, System Impedance Monitoring Station, and helped complete the Harmonics Testing Station. While at school, he was able to participate in an internship at Austin Energy, University of Texas Center for Electromagnetics (CEM), and Electric Power Research Institute (EPRI). He was an active member in Tau Beta Pi and Eta Kappa Nu engineering honors societies.

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